KENESAS

RX23W Group **Renesas MCUs**

Datasheet

R01DS0342EJ0100 Rev.1.00 Aug 06, 2019

54-MHz 32-bit RX MCUs, built-in FPU, 88.56 DMIPS, up to 512-KB flash memory, Bluetooth[®] 5.0, various communication functions including USB 2.0 full-speed host/function/OTG, CAN, SD host interface, serial sound interface, capacitive touch sensing unit, 12-bit A/D converter, 12-bit D/A converter, RTC, Encryption functions

Features

32-bit RXv2 CPU core

- Max. operating frequency: 54 MHz Capable of 88.56 DMIPS in operation at 54 MHz
- Enhanced DSP: 32-bit multiply-accumulate and 16-bit
- Built-in FPU: 32-bit single-precision floating point (compliant to provide the providet the p **IEEE754**)
- Divider (fastest instruction execution takes two CPU clock cycles) · Fast interrupt
- CISC Harvard architecture with 5-stage pipeline
- Variable-length instructions, ultra-compact code
- On-chip debugging circuit
- Memory protection unit (MPU) supported
- Low power design and architecture
- Operation from a single 1.8-V to 3.6-V supply
- RTC capable of operating on the battery backup power supply
- Three low power consumption modes
- · Low power timer (LPT) that operates during the software standby state

On-chip flash memory for code

- 384- to 512-Kbyte capacities
- On-board or off-board user programming
- Programmable at 1.8 V
- For instructions and operands

On-chip data flash memory

- 8 Kbytes (1,000,000 program/erase cycles (typ.))
- BGO (Background Operation)
- On-chip SRAM, no wait states

64-Kbyte size capacities Data transfer functions

- DMAC: Incorporates four channels
- DTC: Four transfer modes
- ELC
 - Module operation can be initiated by event signals without using interrupts.
 - Linked operation between modules is possible while the CPU is sleeping.
- Reset and supply management
 - Eight types of reset, including the power-on reset (POR)
 Low voltage detection (LVD) with voltage settings

Clock functions

- Main clock oscillator frequency: 1 to 20 MHz
- · External clock input frequency: Up to 20 MHz
- Sub-clock oscillator frequency: 32.768 kHz
- Frequency of Bluetooth-dedicated clock oscillator: 32 MHz
- PLL circuit input: 4 MHz to 12.5 MHz
 On-chip low- and high-speed oscillators, dedicated on-chip low-speed oscillator for the IWDT
- USB-dedicated PLL circuit: 4, 6, 8, or 12 MHz 54 MHz can be set for the system clock and 48 MHz for the USB clock
- Generation of a dedicated 32.768-kHz clock for the RTC
- Clock frequency accuracy measurement circuit (CAC)

Realtime clock

- Adjustment functions (30 seconds, leap year, and error)
- Calendar count mode or binary count mode selectable
- Time capture function
- Time capture on event-signal input through external pins

Independent watchdog timer

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15-kHz on-chip oscillator produces a dedicated clock signal to drive IWDT operation.

Useful functions for IEC60730 compliance

- Self-diagnostic and disconnection-detection assistance functions for the A/D converter, clock frequency accuracy measurement circuit, independent watchdog timer, RAM test assistance functions using the DOC, etc.
- MPC

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Input/output functions selectable from multiple pins



Up to 12 communication functions

- Bluetooth Low Energy (1 channel) An RF transceiver and link layer compliant with the Bluetooth 5.0 Low
 - Energy specification LE 1M PHY, LE 2M PHY, LE Coded PHY (125 kbps and 500 kbps),
 - and LE Advertising extension support On-chip Bluetooth-dedicated AES-CCM (128-bit blocks) encryption
- circuit • USB 2.0 host/function/On-The-Go (OTG) (one channel),
- full-speed = 12 Mbps, low-speed = 1.5 Mbps, isochronous transfer, and BC (Battery Charger) supported
- CAN (one channel) compliant to ISO11898-1: Transfer at up to 1 Mbps
- SCI with many useful functions (up to 4 channels) Asynchronous mode, clock synchronous mode, smart card interface Reduction of errors in communications using the bit modulation function
- IrDA interface (one channel, in cooperation with the SCI5)
- I²C bus interface: Transfer at up to 400 kbps, capable of SMBus
- operation (one channel) • RSPI (one channel): Transfer at up to 16 Mbps
- Serial sound interface (one channel)
- SD host interface (optional: one channel) SD memory/ SDIO 1-bit or 4-bit SD bus supported

Up to 19 extended-function timers

- 16-bit MTU: input capture, output compare, complementary PWM output, phase counting mode (five channels)
- 16-bit TPU: input capture, output compare, phase counting mode (six channels)
- 8-bit TMR (four channels)
- 16-bit compare-match timers (four channels)
- 12-bit A/D converter
 - Capable of conversion within 0.83 µs
 - 14 channels
 - Sampling time can be set for each channel
 - · Self-diagnostic function and analog input disconnection detection assistance function
- 12-bit D/A converter
- · Two channels

Capacitive touch sensing unit

- · Self-capacitance method: A single pin configures a single key, supporting up to 12 keys
- Mutual capacitance method: Matrix configuration with 12 pins, supporting up to 36 keys

Analog comparator

- Two channels × one unit
- General I/O ports
- 5-V tolerant, open drain, input pull-up, switching of driving capacity
- Encryption functions (TSIP-Lite)
 - · Unauthorized access to the encryption engine is disabled and imposture and falsification of information are prevented
 - Safe management of keys

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- 128- or 256-bit key length of AES for ECB, CBC, GCM, others True random number generator
- Temperature sensor

Applications

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Operating temperature range

· General industrial and consumer equipment

-40 to +85

1. Overview

1.1 Outline of Specifications

 Table 1.1 lists the specifications, and Table 1.2 gives a comparison of the functions of the products in different packages.

Table 1.1 is for products with the greatest number of functions, so the number of peripheral modules and channels will differ in accordance with the package type. For details, see Table 1.2, Comparison of Functions for Different Packages.

Classification	Module/Function	Description			
CPU	• 32-bit RX CPU (RX v2) • Minimum instruction execution time: One instruction per clock cycle • Address space: 4-Gbyte linear • Register set General purpose: Sixteen 32-bit registers Control: Ten 32-bit registers • Basic instructions: 75 (variable-length instruction format) • Floating-point instructions: 11 • DSP instructions: 23 • Addressing modes: 10 • Data arrangement Instructions: Little endian • Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32-bit \rightarrow 32-bit \rightarrow 64-bit • On-chip divider: 32-bit \rightarrow 32-bit • Barrel shifter: 32 bits • Memory protection unit (MPU)				
	FPU	 Single precision (32-bit) floating point Data types and floating-point exceptions in conformance with the IEEE754 standard 			
Memory	ROM	 Capacity: 384/512 Kbytes Up to 32 MHz: No-wait memory access 32 to 54 MHz: Wait state required. No wait state if the instruction is served by a ROM accelerator hit. Programming/erasing method: Serial programming (asynchronous serial communication/USB communication), self-programming 			
	RAM	Capacity: 64 Kbytes54 MHz, no-wait memory access			
	E2 DataFlash	Capacity: 8 KbytesNumber of erase/write cycles: 1,000,000 (typ)			
MCU operating mo	ode	Single-chip mode			
Clock	Clock generation circuit	 Main clock oscillator, sub-clock oscillator, low-speed on-chip oscillator, high-speed on-chip oscillator, PLL frequency synthesizer, USB-dedicated PLL frequency synthesizer, and IWDT-dedicated on-chip oscillator, Bluetooth-dedicated clock oscillator, Bluetooth-dedicated low-speed on-chip oscillator Oscillation stop detection: Available Clock frequency accuracy measurement circuit (CAC) Independent settings for the system clock (ICLK), peripheral module clock (PCLK), and FlashIF clock (FCLK) The CPU and system sections such as other bus masters run in synchronization with the system clock (ICLK): 54 MHz (at max.) MTU2a runs in synchronization with the PCLKA: 54 MHz (at max.) Peripheral modules other than MTU2a and S12ADE run in synchronization with the PCLKB: 32 MHz (at max.) The flash peripheral circuit runs in synchronization with the FCLK: 32 MHz (at max.) 			
Resets		RES# pin reset, power-on reset, voltage monitoring reset, watchdog timer reset, independent watchdog timer reset, and software reset			
Voltage detection	Voltage detection circuit (LVDAb)	 When the voltage on VCC falls below the voltage detection level, an internal reset or internal interrupt is generated. Voltage detection circuit 0 is capable of selecting the detection voltage from 3 levels Voltage detection circuit 1 is capable of selecting the detection voltage from 10 levels 			

Table 1.1Outline of Specifications (1/4)



Classification	Module/Function	Description				
Low power consumption	Low power consumption functions	 Module stop function Three low power consumption modes Sleep mode, deep sleep mode, and software standby mode Low power timer that operates during the software standby state 				
	Function for lower operating power consumption	 Operating power control modes High-speed operating mode, middle-speed operating mode, and low-speed operating mode 				
Interrupt	Interrupt controller (ICUb)	 Interrupt vectors: 148 External interrupts: 7 (NMI, IRQ0, IRQ1, IRQ4 to IRQ7 pins) Non-maskable interrupts: 6 (NMI pin, oscillation stop detection interrupt, voltage monitoring 1 interrupt, WDT interrupt, IWDT interrupt, and VBATT power monitoring interrupt) 16 levels specifiable for the order of priority 				
DMA	DMA controller (DMACA)	 4 channels Three transfer modes: Normal transfer, repeat transfer, and block transfer Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions 				
	Data transfer controller (DTCa)	 Transfer modes: Normal transfer, repeat transfer, and block transfer Activation sources: Interrupts Chain transfer function 				
I/O ports	General I/O ports	85-pin/56-pin I/O: 43/29 • Input: 1/1 Pull-up resistors: 43/29 • Open-drain outputs: 31/24 • 5-V tolerance: 5/4				
Event link controller (ELC)		 Event signals of 59 types can be directly connected to the module Operations of timer modules are selectable at event input Capable of event link operation for port B and port E 				
Multi-function pin c	controller (MPC)	Capable of selecting the input/output function from multiple pins				
Timers	16-bit timer pulse unit (TPUa)	 (16 bits × 6 channels) × 1 unit Maximum of 10 pulse-input/output possible Select from among seven or eight counter-input clock signals for each channel Supports the input capture/output compare function Output of PWM waveforms in up to 9 phases in PWM mode Support for buffered operation, phase-counting mode (two-phase encoder input) and cascade connected operation (32 bits × 2 channels) depending on the channel. Capable of generating conversion start triggers for the A/D converters Signals from the input capture pins are input via a digital filter Clock frequency measuring method 				
	Multi-function timer pulse unit 2 (MTU2a)	 (16 bits × 5 channels) × 1 unit Up to 15 pulse-input/output lines are available based on the six 16-bit timer channels Select from among eight or seven counter-input clock signals for each channel (PCLK/1, PCLK/4, PCLK/16, PCLK/64, PCLK/256, PCLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD). Input capture function 18 output compare/input capture registers Pulse output mode Reset synchronous PWM mode Phase-counting mode Capable of generating conversion start triggers for the A/D converter 				
	Port output enable 2 (POE2a)	Controls the high-impedance state of the MTU's waveform output pins				
	Compare match timer (CMT)	 (16 bits × 2 channels) × 2 units Select from among four clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512) 				
	Watchdog timer (WDTA)	 14 bits × 1 channel Select from among six counter-input clock signals (PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192) 				

Table 1.1Outline of Specifications (2/4)

Classification	Module/Function	Description
Timers	Independent watchdog timer (IWDTa)	 14 bits × 1 channel Count clock: Dedicated low-speed on-chip oscillator for the IWDT Frequency divided by 1, 16, 32, 64, 128, or 256
	Realtime clock (RTCe)	 Clock source: Sub-clock Time/calendar Interrupts: Alarm interrupt, periodic interrupt, and carry interrupt Time-capture facility for two values
	Low power timer (LPT)	 16 bits × 1 channel Clock source: Sub-clock, Dedicated low-speed on-chip oscillator for the IWDT Frequency divided by 2, 4, 8, 16, or 32
	8-bit timer (TMR)	 (8 bits × 2 channels) × 2 units Seven internal clocks (PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, and PCLK/8192) and an external clock can be selected Pulse output and PWM output with any duty cycle are available Two channels can be cascaded and used as a 16-bit timer
Communication functions	Serial communications interfaces (SCIg, SCIh)	 4 channels (channel 1, 5, 8: SClg, channel 12: SClh) SClg Serial communications modes: Asynchronous, clock synchronous, and smart-card interface Multi-processor function On-chip baud rate generator allows selection of the desired bit rate Choice of LSB-first or MSB-first transfer Average transfer rate clock can be input from TMR timers for SCl5, and SCl12 Start-bit detection: Level or edge detection is selectable. Simple I²C Simple SPI 9-bit transfer mode Bit rate modulation Event linking by the ELC (only on channel 5) SCIh (The following functions are added to SClg) Supports the serial communications protocol, which contains the start frame and information frame Supports the LIN format
	IrDA interface (IRDA)	 1 channel (SCI5 used) Supports encoding/decoding of waveforms conforming to IrDA standard 1.0
	I ² C bus interface (RIICa)	 1 channel Communications formats: I²C bus format/SMBus format Master mode or slave mode selectable Supports fast mode
	Serial peripheral interface (RSPIa)	 1 channel Transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) Capable of handling serial transfer as a master or slave Data formats Choice of LSB-first or MSB-first transfer The number of bits in each transfer can be changed to 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) Double buffers for both transmission and reception
	USB 2.0 host/function module (USBc)	 USB Device Controller (UDC) and transceiver for USB 2.0 are incorporated. Host/function module: 1 port Compliant with USB version 2.0 Transfer speed: Full-speed (12 Mbps), low-speed (1.5 Mbps) OTG (ON-The-Go) is supported. Isochronous transfer is supported. BC1.2 (Battery Charging Specification Revision 1.2) is supported.
	CAN module (RSCAN)	 1 channel Compliance with the ISO11898-1 specification (standard frame and extended frame) 16 Message boxes

Table 1.1Outline of Specifications (3/4)



Classification	Module/Function	Description
Communication functions	Serial Sound Interface (SSI) SD Host Interface (SDHIa)	 1 channel Capable of duplex communications Various serial audio formats supported Master/slave function supported Programmable word clock or bit clock generation function 8/16/18/20/22/24/32-bit data formats supported On-chip 8-stage FIFO for transmission/reception Supports WS continue mode in which the SSIWS signal is not stopped. 1 channel Transfer speed: Default speed mode (8MB/s) SD memory card interface (1 bit / 4bits SD bus)
		 MMC, eMMC Backward-compatible are supported. SD Specifications Part 1: Compliant with Physical Layer Specification Ver.3.01 (Not support DDR) Part E1: SDIO Specification Ver. 3.00 Error check function: CRC7 (command), CRC16 (data) Interrupt Source: Card access interrupt, SDIO access interrupt, Card detection interrupt, SD buffer access interrupt DMA transfer sources: SD_BUF write, SD_BUF read Card detection, Write protection
	Bluetooth low energy (BLE)	 On-chip RF transceiver and link layer compliant with the Bluetooth 5.0 Low Energy specification Bit rates: 1 Mbps, 2 Mbps, 500 kbps, and 125 kbps LE Advertising extension support Includes an RF transceiver power supply (selectable as a DC-to-DC converter or linear regulator) On-chip matching circuit to help reduce the number of external parts Transmission power: +4 dBm support
Encryption functio	ns	 Access management circuit Encryption engine 128- or 256-bit key sizes of AES Block cipher mode of operation: GCM, ECB, CBC, CMAC, XTS, CTR, GCTR Hash function True random number generator Prevention from illicit copying of a key
12-bit A/D convert	er (S12ADE)	 12 bits (14 channels × 1 unit) 12-bit resolution Minimum conversion time: 0.83 µs per channel when the ADCLK is operating at 54 MHz Operating modes Scan mode (single scan mode, continuous scan mode, and group scan mode) Group A priority control (only for group scan mode) Sampling variable Sampling time can be set up for each channel. Self-diagnostic function Double trigger mode (A/D conversion data duplicated) Detection of analog input disconnection A/D conversion start conditions A software trigger, a trigger from a timer (MTU, TPU), an external trigger signal, or ELC Event linking by the ELC
Temperature sens	or (TEMPSA)	 1 channel The voltage output from the temperature sensor is converted into a digital value by the 12-bit A/D converter.
12-bit D/A convert	er (R12DAA)	 2 channels 12-bit resolution Output voltage: 0.4 to AVCC0-0.5V
CRC calculator (C	RC)	 CRC code generation for arbitrary amounts of data in 8-bit units Select any of three generating polynomials: X⁸ + X² + X + 1, X¹⁶ + X¹⁵ + X² + 1, or X¹⁶ + X¹² + X⁵ + 1 Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.
Comparator B (CM	IPBa)	 2 channels × 1 unit Function to compare the reference voltage and the analog input voltage Window comparator operation or standard comparator operation is selectable
Capacitive touch s	ensing unit (CTSU)	Detection pin: 12 channels
Data operation cire	cuit (DOC)	Comparison, addition, and subtraction of 16-bit data
Power supply volta	ages/Operating frequencies	VCC = 1.8 to 2.4 V: 8 MHz, VCC = 2.4 to 2.7 V: 16 MHz, VCC = 2.7 to 3.6 V: 54 MHz
Operating tempera	ature range	D version: -40 to +85°C
Packages		85-pin BGA (PTBG0085KB-A) 5.5 × 5.5 mm, 0.5 mm pitch 56-pin QFN (PVQN0056LA-A) 7 × 7 mm, 0.4 mm pitch
Debugging interfa	ces	FINE interface

Table 1.1Outline of Specifications (4/4)



		RX23W Group			
Module/Functions		85 Pins 56 Pins			
External bus	External bus	Not su	oported		
Interrupts	External interrupts	NMI, IRQ0, IRQ	1, IRQ4 to IRQ7		
DMA	DMA controller	4 channels (DM	AC0 to DMAC3)		
	Data transfer controller	Avai	lable		
Timers	16-bit timer pulse unit	6 channels (TPU0 to TPU5)	5 channels (TPU0 to TPU3, TPU5)		
	Multi-function timer pulse unit 2	5 channels (M	TU0 to MTU4)		
	Port output enable 2	POE0#, POE1#, POE3#, POE8#	POE0#, POE8#		
	8-bit timer	2 channel	s × 2 units		
	Compare match timer	2 channel	s × 2 units		
	Low power timer	1 cha	annel		
	Realtime clock	Avai	lable		
	Watchdog timer	Avai	lable		
	Independent watchdog timer	Avai	lable		
Communication functions	Serial communications interfaces (SCIg)	3 channels (SCI1, 5, 8)			
	IrDA interface	1 chann	el (SCI5)		
	Serial communications interfaces (SCIh)	1 channel (SCI12)	Not supported		
	I ² C bus interface	1 cha	annel		
	CAN module	1 cha	annel		
	Serial peripheral interface	1 cha	annel		
	USB 2.0 host/function module	1 cha	annel		
	Serial sound interface	1 cha	annel		
	SD Host Interface	1 channel	Not supported		
	Bluetooth low energy	An RF transceiver and link layer energy sp	compliant with Bluetooth 5.0 low ecification		
Capacitive touch sensing u	unit	12 channels	9 channels		
12-bit A/D converter (inclu	ding high-precision channels)	14 channels (8 channels) 8 channels (4 channel			
Temperature sensor		Available			
D/A converter		2 channels	1 channel		
CRC calculator		Available			
Event link controller		Available			
Comparator B		2 cha	annels		
Packages		85-pin BGA	56-pin QFN		

Table 1.2 Comparison of Functions for Different Packages



1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no., memory capacity, and package type.

Group	Part No.	Order Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operationg Frequency	Scurity Function	Operating Temperature
RX23W	R5F523W8ADBL	R5F523W8ADBL#20	PTBG0085KB-A	512 Kbytes	64 Kbytes	8 Kbytes	54 MHz	Not available	–40 to +85°C
	R5F523W8ADNG	R5F523W8ADNG#30	PVQN0056LA-A					Not available	
	R5F523W8BDBL	R5F523W8BDBL#20	PTBG0085KB-A					Available	
	R5F523W8BDNG	R5F523W8BDNG#30	PVQN0056LA-A					Available	
	R5F523W7ADBL	R5F523W7ADBL#20	PTBG0085KB-A	384 Kbytes				Not available	
	R5F523W7ADNG	R5F523W7ADNG#30	PVQN0056LA-A					Not available	
	R5F523W7BDBL	R5F523W7BDBL#20	PTBG0085KB-A					Available	
	R5F523W7BDNG	R5F523W7BDNG#30	PVQN0056LA-A					Available	

Table 1.3 List of Products: D Version (T_a = -40 to +85°C)





1.3 Block Diagram

Figure 1.2 shows a block diagram.

SDHIa RSCAN CTSU	E2 DataFlash WDTA
LPT	ELC
	SClg × 3 channels (including IrDA × 1 channel)
	SCIh × 1 channel
	RSPla × 1 channel
	RIICa × 1 channel
	SSI
	USB 2.0 host/function module
	TPUa × 6 channels
	MTU2a × 5 channels
	POE2a
	TMR × 2 channels (unit 0)
	TMR × 2 channels (unit 1)
	CMT × 2 channels (unit 0)
	CMT × 2 channels (unit 1)
	RTCe Port 2
	12-bit A/D converter × 14 channels Port 3
	Temperature sensor Port 4
	12-bit D/A converter × 2 channels
	DOC Bot C
	Comparator B × 2 channels
	BLE
generation	Port J
ICUb: Interrupt controller DTCa: Data transfer controller DMACA: DMA controller WDTA: Watchdog timer IWDTa: Independent watchdog timer ELC: Event link controller CRC: CRC (cyclic redundancy check) calculator SCIg/SCIh: Serial communications interface RSPIa: Serial peripheral interface RIIC: I ² C bus interface SSI: Serial sound interface TPUa: 16-bit timer pulse unit MTU2a: Multi-function timer pulse unit 2	POE2a: Port output enable 2 TMR: 8-bit timer CMT: Compare match timer RTCe: Realtime clock DOC: Data operation circuit CAC: Clock frequency accuracy measurement circuit BLE: Bluetooth Low Energy SDHIa: SD host interface RSCAN: CAN module CTSU: Capacitive touch sensing unit LPT: Low power timer MPU: Memory protection unit
Figure 1.2 Block Diagram	



1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4Pin Functions (1/4)

Classifications	Pin Name	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply.
	VCL	—	Connect this pin to the VSS pin via a 4.7 μ F smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
	VBATT	Input	Backup power pin
Clock	XTAL	Output	Pins for connecting a crystal. An external clock can be input through the
	EXTAL	Input	EXTAL pin.
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal between
	XCOUT	Output	XCIN and XCOUT.
	CLKOUT_RF	Output	Bluetooth-dedicated clock output pin for output of a 1-, 2-, or 4-MHz signal
	XTAL1_RF	Input	Pins for connecting the Bluetooth-dedicated clock oscillator. Connect a 32-
	XTAL2_RF	Output	MHz oscillator to these pins.
	CLKOUT	Output	Clock output pin.
Operating mode control	MD	Input	Pin for setting the operating mode. The signal levels on this pin must not be changed during operation.
	UB	Input	Pin used for boot mode (USB interface).
	UPSEL	Input	Pin used for boot mode (USB interface).
System control	RES#	Input	Reset pin. This MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Input pin for the clock frequency accuracy measurement circuit.
On-chip emulator	FINED	I/O	FINE interface pin.
Interrupts	NMI	Input	Non-maskable interrupt request pin.
	IRQ0, IRQ1, IRQ4 to IRQ7	Input	Interrupt request pins.
16-bit timer	TIOCB0	I/O	The TGRB0 inputs capture input/output compare output/PWM output pins.
pulse unit	TIOCB1	I/O	The TGRB1 inputs capture input/output compare output/PWM output pins.
	TIOCB2	I/O	The TGRB2 inputs capture input/output compare output/PWM output pins.
	TIOCA3, TIOCB3, TIOCC3, TIOCD3	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins.
	TIOCA4, TIOCB4	I/O	The TGRA4 and TGRB4 input capture input/output compare output/PWM output pins.
	TIOCB5	I/O	The TGRB5 inputs capture input/output compare output/PWM output pins.
	TCLKA, TCLKB, TCLKC, TCLKD	Input	Input pins for external clock signals.
Multi-function timer pulse unit 2	MTIOC0A, MTIOC0B, MTIOC0C	I/O	The TGRA0 to TGRC0 input capture input/output compare output/PWM output pins.
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins.
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins.
	MTIOC3A, MTIOC3B, MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins.
	MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins.
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	Input pins for the external clock.



Classifications	Pin Name	I/O	Description		
Port output enable 2	POE0#, POE1#, POE3#, POE8#	Input	Input pins for request signals to place the MTU pins in the high impedance state.		
Realtime clock	RTCOUT	Output	Output pin for the 1-Hz/64-Hz clock.		
	RTCIC0, RTCIC1	Input	Time capture event input pins.		
8-bit timer	TMO0 to TMO2	Output	Compare match output pins.		
	TMCI0 to TMCI3	Input	Input pins for the external clock to be input to the counter.		
	TMRI1 to TMRI3	Input	Counter reset input pins.		
Serial	Asynchronous mode/clock s	synchrono	us mode		
communications	SCK1, SCK5, SCK8	I/O	Input/output pins for the clock.		
interface (Colg)	RXD1, RXD5, RXD8	Input	Input pins for received data.		
	TXD1, TXD5, TXD8	Output	t Output pins for transmitted data.		
	CTS1#, CTS5#, CTS8#	Input	Input pins for controlling the start of transmission and reception.		
	RTS1#, RTS5#, RTS8#	Output	Output pins for controlling the start of transmission and reception.		
	Simple I ² C mode				
	SSCL1, SSCL5, SSCL8	I/O	Input/output pins for the I ² C clock.		
	SSDA1, SSDA5, SSDA8	I/O	Input/output pins for the I ² C data.		
	Simple SPI mode				
	SCK1, SCK5, SCK8	, SCK5, SCK8 I/O Input/output pins for the clock.			
	SMISO1, SMISO5, SMISO8	I/O	Input/output pins for slave transmit data.		
	SMOSI1, SMOSI5, SMOSI8	I/O	Input/output pins for master transmit data.		
	SS1#, SS5#, SS8#	Input	Slave-select input pins.		
IrDA interface	IRTXD5	Output	Data output pin in the IrDA format.		
	IRRXD5	Input	Data input pin in the IrDA format.		
Serial	Asynchronous mode/clock s	synchrono	us mode		
communications	SCK12	I/O	Input/output pin for the clock.		
	RXD12	Input	Input pin for receiving data.		
	TXD12	Output	Output pin for transmitting data.		
	CTS12#	Input	Input pin for controlling the start of transmission and reception.		
	RTS12#	Output	Output pin for controlling the start of transmission and reception.		
	Simple I ² C mode				
	SSCL12	I/O	Input/output pin for the I ² C clock.		
	SSDA12	I/O	Input/output pin for the I ² C data.		
	Simple SPI mode				
	SCK12	I/O	Input/output pin for the clock.		
	SMISO12	I/O	Input/output pin for slave transmit data.		
	SMOSI12	I/O	Input/output pin for master transmit data.		
	SS12#	Input	Slave-select input pin.		
	 Extended serial mode 				
	RXDX12	Input	Input pin for data reception by SCIf.		
	TXDX12	Output	Output pin for data transmission by SCIf.		
	SIOX12	I/O	Input/output pin for data reception or transmission by SCIf.		
l ² C bus interface	SCL	I/O	Input/output pin for I ² C bus interface clocks. Bus can be directly driven by the N-channel open drain output.		
	SDA	I/O	Input/output pin for I ² C bus interface data. Bus can be directly driven by the N-channel open drain output.		

Table 1.4Pin Functions (2/4)



	()				
Classifications	Pin Name	I/O	Description		
Serial peripheral	RSPCKA	I/O	Input/output pin for the RSPI clock.		
Interface	MOSIA	I/O	Input/output pin for transmitting data from the RSPI master.		
	MISOA	I/O	Input/output pin for transmitting data from the RSPI slave.		
	SSLA0	I/O	Input/output pin to select the slave for the RSPI.		
	SSLA1, SSLA3	Output	Output pins to select the slave for the RSPI.		
Serial sound	SSISCK0	I/O	SSI serial bit clock pin.		
interface	SSIWS0	I/O	Word selection pin.		
	SSITXD0	Output	Serial data output pin.		
	SSIRXD0	Input	Serial data input pin.		
	AUDIO_MCLK	Input	Master clock pin for audio.		
CAN module	CRXD0	Input	Input pin		
	CTXD0	Output	Output pin		
SD host	SDHI_CLK	Output	SD clock output pin		
interface	SDHI_CMD	I/O	SD command output, response input signal pin		
	SDHI_D3 to SDHI_D0	I/O	SD data bus pins		
	SDHI_CD	Input	SD card detection pin		
	SDHI_WP	Input	SD write-protect signal		
USB 2.0 host/ function module	VCC_USB	Input	Power supply pin for USB. Connect this pin to VCC or connect this pin VSS via a $0.33 \ \mu$ F smoothing capacitor for stabilizing the internal powe supply.		
	VSS_USB	Input	Ground pin for USB. Connect this pin to VSS.		
	USB0_DP	I/O	D+ I/O pin of the USB on-chip transceiver.		
	USB0_DM	I/O	D- I/O pin of the USB on-chip transceiver.		
	USB0_VBUS	Input	USB cable connection monitor pin.		
	USB0_EXICEN	Output	Low-power control signal for the OTG chip.		
	USB0_VBUSEN	Output	VBUS (5 V) supply enable signal for the OTG chip.		
	USB0_OVRCURA, USB0_OVRCURB	Input	External overcurrent detection pins.		
	USB0_ID	Input	Mini-AB connector ID input pin during operation in OTG mode.		
12-bit A/D converter	AN000 to AN007, AN016 to AN020, AN027	Input	Input pins for the analog signals to be processed by the A/D converter.		
	ADTRG0#	Input	Input pin for the external trigger signal that start the A/D conversion.		
12-bit D/A converter	DA0, DA1	Output	Analog output pins of the D/A converter.		
Comparator B	CMPB2, CMPB3	Input	Input pin for the analog signal to be processed by comparator B.		
	CVREFB2, CVREFB3	Input	Analog reference voltage supply pin for comparator B.		
	CMPOB2, CMPOB3	Output	Output pin for comparator B.		
CTSU	TS2 to TS4, TS7, TS8, TS12, TS13, TS22, TS23, TS27, TS30, TS35	Output	Electrostatic capacitance measurement pins (touch pins).		
	TSCAP	Output	LPF connection pin.		
Analog power supply	AVCC0	Input	Analog voltage supply pin for the 12-bit A/D converter and D/A converter. Connect this pin to VCC when not using the 12-bit A/D converter and D/A converter.		
	AVSS0	Input	Analog ground pin for the 12-bit A/D converter and D/A converter. Connect this pin to VSS when not using the 12-bit A/D converter and D/A converter.		
	VREFH0	Input	Analog reference voltage supply pin for the 12-bit A/D converter.		
	VREFL0	Input	Analog reference ground pin for the 12-bit A/D converter.		

Table 1.4Pin Functions (3/4)



Classifications	Pin Name	I/O	Description
I/O ports	P03, P05, P07	I/O	3-bit input/output pins.
	P14 to P17	I/O	4-bit input/output pins.
	P21, P22, P25 to P27	I/O	5-bit input/output pins.
	P30, P31, P35 to P37	I/O	5-bit input/output pins (P35 input pin).
	P40 to P47	I/O	8-bit input/output pins.
	PB0, PB1, PB3, PB5, PB7	I/O	5-bit input/output pins.
	PC0, PC2 to PC7	I/O	7-bit input/output pins.
	PD3	I/O	1-bit input/output pins.
	PE0 to PE4	I/O	5-bit input/output pins.
	PJ3	I/O	1-bit input/output pin.
Bluetooth low energy	ANT	I/O	RF single I/O pin for RF transceiver Set the impedance of the signal line to 50 Ω .
	DCLOUT	Output	RF transceiver power-supply output pin
	DCLIN_A	Input	RF transceiver power-supply output connection pin
	DCLIN_D	Input	RF transceiver power-supply output connection pin
	VCC_RF	Input	RF transceiver power supply pin
	AVCC_RF	Input	RF transceiver power supply pin
	VSS_RF	Input	RF transceiver ground pin

Table 1.4Pin Functions (4/4)



1.5 Pin Assignments

Figure 1.3 and Figure 1.4 show the pin assignments. Table 1.5 and Table 1.6 show the lists of pins and pin functions.



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Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, RIIC, RSCAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
A1		P25	MTIOC4C/MTCLKB/TIOCA4			TS4	ADTRG0#
A2		P30	MTIOC4B/TMRI3/POE8#/ RTCIC0	RXD1/SMISO1/SSCL1/ AUDIO_MCLK			IRQ0/CMPOB3
A3	VCC						
A4	EXTAL	P36					
A5	VSS						
A6	XTAL	P37					
A7	XCOUT						
A8	XCIN						
A9	VCL						
A10	AVSS0						
B1		P17	MTIOC3A/MTIOC3B/TMO1/ POE8#/TIOCB0/TCLKD	SCK1/MISOA/SDA/SSITXD0			IRQ7/CMPOB2
B2		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1/SSIRXD0/ USB0_VBUSEN		TS3	CMPB3
B3		P27	MTIOC2B/TMCI3	SCK1/SSIWS0		TS2	CVREFB3
B4		P31	MTIOC4D/TMCI2/RTCIC1	CTS1#/RTS1#/SS1#/SSISCK0			IRQ1
B5	UPSEL	P35					NMI
B6	RES#						
B7	MD						FINED
B8		P03					DA0
B9		P05					DA1
B10	AVCC0						
C1		P14	MTIOC3A/MTCLKA/TMRI2/ TIOCB5/TCLKA	CTS1#/RTS1#/SS1#/CTXD0/ USB0_OVRCURA		TS13	IRQ4/ CVREFB2
C2		P15	MTIOC0B/MTCLKB/TMCI2/ TIOCB2/TCLKB	RXD1/SMISO1/SSCL1/CRXD0		TS12	IRQ5/CMPB2
C3		P16	MTIOC3C/MTIOC3D/TMO2/ TIOCB1/TCLKC/RTCOUT	TXD1/SMOSI1/SSDA1/MOSIA/SCL/ USB0_VBUS/USB0_VBUSEN/ USB0_OVRCURB			IRQ6/ ADTRG0#
C4		P22	MTIOC3B/MTCLKC/TMO0/ TIOCC3	USB0_OVRCURB/AUDIO_MCLK		TS7	
C5	VBATT						
C6		PJ3	MTIOC3C				
C7		P07					ADTRG0#
C8		P41					AN001
C9		P40					AN000
C10	VREFH0						
D1				USB0_DM			
D2	VCC_USB						
D3		P21	MTIOC1B/TMCI0/TIOCA3	USB0_EXICEN/SSIWS0		TS8	
D4	VSS_RF						
D8		P42					AN002
D9		P43					AN003
D10	VREFL0						
E1				USB0_DP			
E2	VSS_USB						
E3	VSS_RF						ļ
E8		P46					AN006
E9		P45					AN005
E10		P44					AN004
F1	UB	PC7	MTIOC3A/MTCLKB/TMO2	TXD8/SMOSI8/SSDA8/MISOA			CACREF
F2		PC6	MTIOC3C/MTCLKA/TMCI2	RXD8/SMISO8/SSCL8/MOSIA/ USB0_EXICEN		TS22	
F3	VSS_RF						
F8	VSS_RF						

Table 1.5 List of Pins and Pin Functions (85-Pin BGA) (1/2)



Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, RIIC, RSCAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
F9		PD3	POE8#				AN027
F10		P47					AN007/ CLKOUT_RF
G1		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	CTS8#/RTS8#/SS8#/SSLA0/SCK5	SDHI_D1	TSCAP	
G2		PC5	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA/USB0_ID		TS23	
G3	VSS_RF						
G8	VSS_RF						
G9		PE0		SCK12			AN016
G10	DCLIN_A						
H1		PC3	MTIOC4D/TCLKB	TXD5/SMOSI5/SSDA5/IRTXD5	SDHI_D0	TS27	
H2		PC2	MTIOC4B/TCLKA	RXD5/SMISO5/SSCL5/SSLA3/ IRRXD5	SDHI_D3	TS30	
H3	VSS_RF						
H4		PB3	MTIOC0A/MTIOC4A/TMO0/ POE3#/TIOCD3/TCLKD		SDHI_WP		
H5	VSS_RF						
H6	VSS_RF						
H7	VSS_RF						
H8		PE3	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#/ AUDIO_MCLK			AN019/ CLKOUT
H9		PE2	MTIOC4A	RXD12/RXDX12/SMISO12/SSCL12			IRQ7/AN018
H10	DCLIN_D						
J1		PC0	MTIOC3C/TCLKC	CTS5#/RTS5#/SS5#/SSLA1		TS35	
J2	VSS_RF						
J3		PB7	MTIOC3B/TIOCB5		SDHI_D2		
J4		PB5	MTIOC2A/MTIOC1B/TMRI1/ POE1#/TIOCB4	USB0_VBUS	SDHI_CD		
J5		PB1	MTIOC0C/MTIOC4C/TMCI0/ TIOCB3		SDHI_CLK		IRQ4
J6		PB0	TIOCA3	RSPCKA	SDHI_CMD		
J7	VSS_RF						
J8		PE4	MTIOC4D/MTIOC1A				AN020/ CLKOUT
J9		PE1	MTIOC4C	TXD12/TXDX12/SIOX12/SMOSI12/ SSDA12			AN017
J10	VCC_RF						
K1	VSS_RF						
K2							ANT
K3	VSS_RF						
K4	VCC						
K5	VSS						
K6	XTAL2_RF						
K7	XTAL1_RF						
K8	AVCC_RF						
K9	DCLOUT						
K10	VSS_RF						

Table 1.5	List of Pins and Pin Functions (85-Pin BGA) (2/2)

1

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, RIIC, RSCAN, USB, SSI)	Touch sensing	Others
1	VCL					
2	MD					FINED
3	XCIN					
4	XCOUT					
5	RES#					
6	XTAL	P37				
7	VSS					
8	EXTAL	P36				
9	VCC					
10	UPSEL	P35				NMI
11		P31	MTIOC4D/TMCI2/RTCIC1	CTS1#/RTS1#/SS1#/SSISCK0		IRQ1
12		P30	MTIOC4B/TMRI3/POE8#/RTCIC0	RXD1/SMISO1/SSCL1/AUDIO_MCLK		IRQ0/CMPOB3
13		P27	MTIOC2B/TMCI3	SCK1/SSIWS0	TS2	CVREFB3
14		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1/SSIRXD0/ USB0_VBUSEN	TS3	CMPB3
15		P17	MTIOC3A/MTIOC3B/TMO1/POE8#/ TIOCB0/TCLKD	SCK1/MISOA/SDA/SSITXD0		IRQ7/CMPOB2
16		P16	MTIOC3C/MTIOC3D/TMO2/TIOCB1/ TCLKC/RTCOUT	TXD1/SMOSI1/SSDA1/MOSIA/SCL/ USB0_VBUS/USB0_VBUSEN/ USB0_OVRCURB		IRQ6/ADTRG0#
17		P15	MTIOC0B/MTCLKB/TMCI2/TIOCB2/ TCLKB	RXD1/SMISO1/SSCL1/CRXD0	TS12	IRQ5/CMPB2
18		P14	MTIOC3A/MTCLKA/TMRI2/TIOCB5/ TCLKA	CTS1#/RTS1#/SS1#/CTXD0/ USB0_OVRCURA	TS13	IRQ4/CVREFB2
19	VCC_USB					
20				USB0_DM		
21				USB0_DP		
22	VSS_USB					
23	UB	PC7	MTIOC3A/MTCLKB/TMO2	TXD8/SMOSI8/SSDA8/MISOA		CACREF
24		PC6	MTIOC3C/MTCLKA/TMCI2	RXD8/SMISO8/SSCL8/MOSIA/ USB0_EXICEN	TS22	
25		PC5	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA/USB0_ID	TS23	
26		PC4	MTIOC3D/MTCLKC/TMCI1/POE0#	CTS8#/RTS8#/SS8#/SSLA0/SCK5	TSCAP	
27		PC3	MTIOC4D/TCLKB	TXD5/SMOSI5/SSDA5/IRTXD5	TS27	
28	VSS_RF					
29		PC2	MTIOC4B/TCLKA	RXD5/SMISO5/SSCL5/SSLA3/IRRXD5	TS30	
30		PC0	MTIOC3C/TCLKC	CTS5#/RTS5#/SS5#/SSLA1	TS35	
31		PB7	MTIOC3B/TIOCB5			
32						ANT
33		PB1	MTIOC0C/MTIOC4C/TMCI0/TIOCB3			IRQ4
34	VCC					
35		PB0	TIOCA3	RSPCKA		
36	VSS					
37	XTAL2_RF					ļ
38	XTAL1_RF					
39	AVCC_RF					
40	DCLOUT					
41		PE4	MTIOC4D/MTIOC1A			AN020/CLKOUT
42		PE3	MTIOC4B/POE8#	AUDIO_MCLK		AN019/CLKOUT
43	1/00 FF	PE2	MTIOC4A			IRQ7/AN018
44	VCC_RF					
45	DCLIN_D					
46	DCLIN_A	DDA	D050#			41007
4/		PD3	PUE8#		<u> </u>	AN027
48		P47				CLKOUT_RF

Table 1.6	List of Pins and Pin Functions (56-PinQFN) (1/2)



Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, RIIC, RSCAN, USB, SSI)	Touch sensing	Others
49		P46				AN006
50		P45				AN005
51		P41				AN001
52	VREFL0					
53	VREFH0					
54	AVCC0					
55		P05				DA1
56	AVSS0					

Table 1.6List of Pins and Pin Functions (56-PinQFN) (2/2)

Note: VSS_RF is assigned as the exposed die pad. For details, refer to Appendix 2, Package Dimensions.



2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2.1 Absolute Maximum Ratings

Conditions: VSS = AVSS0 = VREFL0 = VREFL = VSS_USB = VSS_RF = 0 V

	Item	Symbol	Value	Unit
Power supply vo	oltage	VCC, VCC_USB	-0.3 to +4.0	V
VBATT power s	upply voltage	VBATT	-0.3 to +4.0	V
Input voltage	Ports for 5 V tolerant*1	V _{in}	-0.3 to +6.5	V
	P03, P05, P07, P40 to P47		-0.3 to AVCC0 + 0.3	
	ANT		-1.0 to +1.4	
	XTAL1_RF, XTAL2_RF		-0.3 to +1.4	
	DCLIN_A, DCLIN_D		–0.3 to +2.2	
	Ports other than above		-0.3 to VCC + 0.3	
Reference powe	er supply voltage	VREFH0	-0.3 to AVCC0 + 0.3	V
Analog power si	upply voltage	AVCC0	-0.3 to +4.0	V
		VCC_RF	-0.3 to +4.0	V
		AVCC_RF	-0.3 to +4.0	V
Analog input	When AN000 to AN007 are used	V _{AN}	-0.3 to AVCC0 + 0.3	V
voltage	When AN016 to AN020, AN027 are used		-0.3 to VCC + 0.3	
Operating tempe	erature	T _{opr}	-40 to +85	°C
Storage temperature		T _{stg}	-55 to +125	°C

Caution: Permanent damage to the MCU may be caused if absolute maximum ratings are exceeded.

To preclude any malfunctions due to noise interference, insert capacitors with high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, between the VCC_USB and VSS_USB pins, between the VREFH0 and VREFL0 pins, between the VCC_RF and VSS_RF pins, and between the AVCC_RF and VSS_RF pins. Place capacitors with values of about 2.2 μ F in the case of the VCC_RF pin and about 0.1 μ F otherwise as close as possible to every power supply pin, and use the shortest and thickest possible traces for the connections.

Connect the VCL pin to a VSS pin via a 4.7 µF capacitor. The capacitor must be placed close to the pin. For details, refer to section 2.16.1, Connecting VCL Capacitor and Bypass Capacitors.

Do not input signals or an I/O pull-up power supply to ports other than 5-V tolerant ports while the device is not powered. The current injection that results from input of such a signal or I/O pull-up may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Even if -0.3 to +6.5 V is input to 5-V tolerant ports, it will not cause problems such as damage to the MCU.

Note 1. Ports 16, 17, 30, 31, and B5 are 5 V tolerant.



Item	Symbol	Conditions Min. Typ. Max.		Unit		
Power supply voltages	VCC*1, *2, *3	When USB is not used	1.8	—	3.6	V
		When USB is used	3.0	—	3.6	
	VSS		—	0	—	
USB power supply voltages	VCC_USB	When USB regulator is not used	—	VCC	—	V
	VSS_USB		—	0	—	
VBATT power supply voltage	VBATT		1.8	—	3.6	V
Analog power supply voltages	AVCC0*1, *2		1.8	—	3.6	V
	AVSS0		—	0	—	
	VREFH0		1.8	—	AVCC0	
	VREFL0		—	0	—	
BLE power supply voltages	VCC_RF ^{*3}		1.8	—	3.6	V
	AVCC_RF*3		1.8	—	3.6	
	VSS_RF		_	0	—	

Table 2.2 Recommended Operating Voltage Conditions

Note 1. P41 and P47: Set AVCC0 to the same voltage as VCC.

If conditions other than those above are applicable, those listed below apply.

While VCC > 2.4 V: AVCC and VCC can be set independently when AVCC0 ≥ 2.4 V

While VCC ≤ 2.4 V: AVCC and VCC can be set independently when AVCC0 ≥ VCC

Note 2. When powering on the VCC and AVCC0 pins, power them on at the same time or the VCC pin first and then the AVCC0 pin.

Note 3. Set VCC_RF and AVCC_RF to the same voltage as VCC.



2.2 DC Characteristics

Table 2.3DC Characteristics (1)

Conditions: $2.7 \text{ V} \le \text{VCC} = \text{VCC}_\text{USB} = \text{VCC}_\text{RF} = \text{AVCC}_\text{RF} \le 3.6 \text{ V}, 2.7 \text{ V} \le \text{AVCC0} \le 3.6 \text{ V}, \text{VSS} = \text{AVSS0} = \text{VSS}_\text{USB} = \text{VSS}_\text{RF} = 0 \text{ V}, \text{ T}_a = -40 \text{ to } +85^{\circ}\text{C}$

Item			Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	RIIC input pin (except for SMBu	ıs, 5 V tolerant)	V _{IH}	VCC × 0.7	_	5.8	V	
	Ports 16, 17, port (5 V tolerant)	t B5		VCC × 0.8	_	5.8		
	Ports 14, 15, port ports 35 to 37, ports B0, B1, B3, ports C0, C2 to C ports D3, ports E0 to E4, port J3, Ports 30, 31 (whe event input is not	ts 21, 22, 25 to 27, B5, B7, 7, en time capture s selected), RES#		VCC × 0.8	_	VCC + 0.3		
	Ports 03, 05, 07,	ports 40 to 47		AVCC0 × 0.8	—	AVCC0 + 0.3		
	Ports 30, 31 (when time	When VCC is supplied		VCC × 0.8	_	VCC + 0.3		
	capture event input is selected)	When VBATT is supplied		VBATT × 0.8		VBATT + 0.3		
	Ports 03, 05, 07,	ports 40 to 47	V _{IL}	-0.3	_	AVCC0 × 0.2		
	RIIC input pin (e)	(cept for SMBus)		-0.3	_	VCC × 0.3		
	Other than RIIC i 30, 31	nput pin or ports		-0.3	_	VCC × 0.2		
	Ports 30, 31 (when time	When VCC is supplied		-0.3	_	VCC × 0.3		
	capture event input is selected)	When VBATT is supplied		-0.3	_	VBATT × 0.3		
	Ports 03, 05, 07,	ports 40 to 47	ΔV_T	AVCC0 × 0.1	_	—		
	RIIC input pin (ex	(cept for SMBus)		VCC × 0.05	_	—		
	Ports 16, 17, Por	t B5		VCC × 0.05	_	—		
	Other than RIIC i	nput pin		VCC × 0.1	_	—		
Input level	MD		V _{IH}	VCC × 0.9	_	VCC + 0.3	V	
voltage (except for Schmitt trigger input	EXTAL (external	clock input)		VCC × 0.8	_	VCC + 0.3		
	RIIC input pin (SI	MBus)		2.1		VCC + 0.3		
pins)	MD		V _{IL}	-0.3		VCC × 0.1		
	EXTAL (external	clock input)		-0.3		VCC × 0.2		
	RIIC input pin (SI	MBus)		-0.3	—	0.8		



Table 2.4DC Characteristics (2)

Conditions: 1.8 V \leq VCC = VCC_USB = VCC_RF = AVCC_RF \leq 2.7 V, 1.8 V \leq AVCC0 < 2.7 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, T_a = -40 to +85°C

Item		Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	Ports 16, 17, port B5 (5 V tolerant)	V _{IH}	VCC × 0.8	_	5.8	V	
	Ports 14, 15, ports 21, 22, 25 to 27, ports 30, 31, 35 to 37, ports B0, B1, B3, B5, B7, ports C0, C2 to C7, ports D3, ports E0 to E4, port J3, RES#		VCC × 0.8	_	VCC + 0.3		
	Ports 03, 05, 07, ports 40 to 47		AVCC0 × 0.8	_	AVCC0 + 0.3		
	Ports 03, 05, 07, ports 40 to 47	V _{IL}	-0.3	-	AVCC0 × 0.2		
	Ports other than above		-0.3	_	VCC × 0.2		
	Ports 03, 05, 07, ports 40 to 47	ΔV_T	AVCC0 × 0.01	_	_		
	Ports other than above		VCC × 0.01	_	_		
Input level	MD	V _{IH}	VCC × 0.9	-	VCC + 0.3	V	
voltage (except	EXTAL (external clock input)		VCC × 0.8	-	VCC + 0.3		
trigger input	MD	V _{IL}	-0.3	_	VCC × 0.1		
pins)	EXTAL (external clock input)		-0.3	_	VCC × 0.2		

Table 2.5DC Characteristics (3)

Conditions: $1.8 \text{ V} \le \text{VCC} = \text{VCC}_{\text{USB}} = \text{AVCC0} = \text{VCC}_{\text{RF}} = \text{AVCC}_{\text{RF}} \le 3.6 \text{ V}, \text{VSS} = \text{AVSS0} = \text{VSS}_{\text{USB}} = \text{VSS}_{\text{RF}} = 0 \text{ V}, \text{T}_{a} = -40 \text{ to } +85^{\circ}\text{C}$

	Symbol	Min.	Тур.	Max.	Unit	Test Conditions		
Input leakage current	RES#, MD, port 35	I _{in}	—	_	1.0	μA	V _{in} = 0 V, VCC	
Three-state leakage current (off-state)	Ports for 5 V tolerant	I _{TSI}	—	_	1.0	μA	V _{in} = 0 V, 5.8 V	
	Ports except for 5 V tolerant		_	-	0.2	μA	V _{in} = 0 V, VCC	
Input capacitance	All input pins (except for port 35, USB0_DM, USB0_DP)	C _{in}	_	_	15	pF	$V_{in} = 0 mV,$ f = 1 MHz, T _a = 25°C	
	Port 35, USB0_DM, USB0_DP			—	30			

Table 2.6DC Characteristics (4)

Conditions: $1.8 V \le VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF \le 3.6 V$, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, $T_a = -40$ to $+85^{\circ}C$

	Symbol	Min.	Тур.	Max.	Unit	Test Conditions	
Input pull-up resistor	All ports (except for port 35)	R _U	10	20	50	kΩ	V _{in} = 0 V



Table 2.7DC Characteristics (5)

Conditions: $1.8 \text{ V} \le \text{VCC} = \text{VCC}_\text{USB} = \text{AVCC0} = \text{VCC}_\text{RF} = \text{AVCC}_\text{RF} \le 3.6 \text{ V}, \text{VSS} = \text{AVSS0} = \text{VSS}_\text{USB} = \text{VSS}_\text{RF} = 0 \text{ V}, \text{T}_a = -40 \text{ to } +85^{\circ}\text{C}$

	Item			Symbol	Typ. *4	Max.	Unit	Test Conditions	
Supply	High-speed	Normal	No peripheral	ICLK = 54 MHz	I _{CC}	6.5	_	mA	
current *1	operating mode	operating mode	operation* ²	ICLK = 32 MHz		4.1	_		
				ICLK = 16 MHz		2.9	_		
				ICLK = 8 MHz		2.2	_		
				ICLK = 4 MHz		1.9	_		
			All peripheral	ICLK = 54 MHz*11		26.5	_		
			operation: Normal	ICLK = 32 MHz*3		21.0	_		
				ICLK = 16 MHz*3		11.8	_		
				ICLK = 8 MHz*3		6.6	_		
				ICLK = 4 MHz*3		4.2	_		
			All peripheral	ICLK = 54 MHz*11		_	53.3		
			operation: Max.	ICLK = 32 MHz*3		_	40.8		
			Increase due to	PCLKB = 32 MHz		_	2		
			operation of the						
		Sloop modo	No poriphoral			3.5			
		Sleep mode	operation*2	ICLK = 32 MHz		2.4			
				ICLK = 16 MHz		1.4			
						1.9			
						1.0			
			All peripheral	ICLK = 54 MHz*11		13.4			
			operation: Normal	ICLK = 32 MHz*3		12.5			
				ICLK = 16 MHz*3		7.3			
				$ICLK = 8 MHz^{*3}$		4.6			
				$ICLK = 4 \text{ MHz}^3$		3.3			
		Deep sleep	No peripheral	ICLK = 54 MHz		2.3			
		mode	operation*2	ICI K = 32 MHz		1.5	_		
				ICLK = 16 MHz		1.3			
				ICLK = 8 MHz		1.2			
				ICLK = 4 MHz		1.1	_		
			All peripheral	ICLK = 54 MHz* ¹¹		10.6	_		
			operation: Normal	ICLK = 32 MHz*3		9.9	_		
				ICLK = 16 MHz*3		5.9	_		
				ICLK = 8 MHz*3		3.8	_		
				ICLK = 4 MHz*3		2.7	_		
		Increase during E	BGO operation* ⁵			2.5			
	Middle-speed	Normal	No peripheral	ICLK = 12 MHz	I _{CC}	2.7	_	mA	
	operating mode	operating mode	operation* ⁶	ICLK = 8 MHz		1.8	_		
				ICLK = 4 MHz		1.4	_		
				ICLK = 1 MHz		1.1	_		
			All peripheral	ICLK = 12 MHz		9.6	_		
			operation: Normal*7	ICLK = 8 MHz		6.2	_	-	
				ICLK = 4 MHz		3.8	—		
				ICLK = 1 MHz		2.3	_		



		Iter	m		Symbol	Typ. *4	Max.	Unit	Test Conditions
Supply current	Middle-speed operating mode	Normal operating mode	All peripheral operation: Max.* ⁷	ICLK = 12 MHz	I _{CC}		16.7	mA	
*1		Sleep mode	No peripheral	ICLK = 12 MHz		1.9	_		
			operation* ⁶	ICLK = 8 MHz		1.2	_		
				ICLK = 4 MHz		1.1	_		
				ICLK = 1 MHz		1.0	_		
			All peripheral	ICLK = 12 MHz		6.1	—		
			operation: Normal*7	ICLK = 8 MHz		4.4	—		
				ICLK = 4 MHz		3.0	—		
				ICLK = 1 MHz		2.0	_		
		Deep sleep	No peripheral	ICLK = 12 MHz		1.6	_		
		mode	operation*6	ICLK = 8 MHz		1.0	_		
				ICLK = 4 MHz		0.9	_		
			ICLK = 1 MHz		0.8	_			
			All peripheral operation: Normal* ⁷	ICLK = 12 MHz		5.1	_		
				ICLK = 8 MHz		3.7	—		
				ICLK = 4 MHz		2.6	_		
				ICLK = 1 MHz		1.8	_		
		Increase during E	3GO operation*5			2.5	_		
	Low-speed operating mode	Normal operating mode	No peripheral operation* ⁸	ICLK = 32 kHz	I _{CC}	5.2	—	μA	
			All peripheral operation: Normal *9, *10	ICLK = 32 kHz		22.3	—		
			All peripheral operation: Max.* ^{9, *10}	ICLK = 32 kHz		_	74.4	-	
		Sleep mode	No peripheral operation* ⁸	ICLK = 32 kHz		3.0			
			All peripheral operation: Normal* ⁹	ICLK = 32 kHz		13.1	—		
		Deep sleep mode	No peripheral operation* ⁸	ICLK = 32 kHz		2.4	—		
			All peripheral operation: Normal* ⁹	ICLK = 32 kHz		10.5	—		

Note 1. Supply current values do not include the output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL. FCLK, and PCLK are set to divided by 64.

Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL. FCLK, and PCLK are the same frequency as that of ICLK.

Note 4. Values when VCC is 3.3 V.

Note 5. This is the increase when data is programmed to or erased from the ROM or E2 DataFlash during program execution.

Note 6. Clock supply to the peripheral functions is stopped. The clock source is PLL when ICLK is 12 MHz and HOCO for other cases. FCLK, and PCLK are set to divided by 64.

Note 7. Clocks are supplied to the peripheral functions. The clock source is PLL when ICLK is 12 MHz and HOCO for other cases. FCLK, and PCLK are the same frequency of that of the ICLK.

Note 8. Clock supply to the peripheral functions is stopped. The clock source is the sub oscillation circuit. FCLK, and PCLK are set to divided by 64.

Note 9. Clocks are supplied to the peripheral functions. The clock source is the sub oscillation circuit. FCLK, and PCLK are the same frequency as that of ICLK.

Note 10. This is the value when the MSTPCRA.MSTPA17 (12-bit A/D converter module stop bit) is in the module stop state.

Note 11. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL. FCLK, and PCLKB are set to divided by 2 and PCLKA and PCLKD are the same frequency as that of ICLK.



Figure 2.1

Voltage Dependency in High-Speed Operating Mode (Reference Data)











Table 2.8DC Characteristics (6)

Conditions: $1.8 V \le VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF \le 3.6 V$, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, $T_a = -40$ to +85°C

ltem			Symbol	Typ.* ³	Max.	Unit	Test Conditions
Supply current*1	Software standby mode* ²	T _a = 25°C	I _{CC}	0.8	3.7	μA	
		T _a = 55°C		1.2	4.3		
		T _a = 85°C		3.5	18.6		
	Increment for IWD		0.4	-			
	Increment for LPT	operation		0.4			Use IWDT-Dedicated On-Chip Oscillator for clock source
	Increment for RTC	Increment for RTC operation*4		0.4	_		RCR3.RTCDV[2:0] set to low drive capacity
				1.2	_		RCR3.RTCDV[2:0] set to normal drive capacity

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.

Note 2. The IWDT, LVD, and CMPB are stopped.

Note 3. When VCC is 3.3 V.

Note 4. This increment includes the oscillation circuit.



Figure 2.4 Voltage Dependency in Software Standby Mode (Reference Data)



Figure 2.5 Temperature Dependency in Software Standby Mode (Reference Data)

Table 2.9DC Characteristics (7)

Conditions: $1.8 \text{ V} \le \text{VCC} = \text{VCC}_{\text{USB}} = \text{AVCC0} = \text{VCC}_{\text{RF}} = \text{AVCC}_{\text{RF}} \le 3.6 \text{ V}, \text{VSS} = \text{AVSS0} = \text{VSS}_{\text{USB}} = \text{VSS}_{\text{RF}} = 0 \text{ V}, \text{T}_{a} = -40 \text{ to } +85^{\circ}\text{C}$

	Item		Symbol	Тур.	Max.	Unit	Test Conditions
Supply	RTC operation	T _a = 25°C	I _{CC}	0.8	_	μA	VBATT = 2.0 V
current*1	when VCC is off	T _a = 55°C		0.9	_		RCR3.RTCDV[2:0] set to low drive capacity
		T _a = 85°C		1.0	_		
		T _a = 25°C		0.9	_		VBATT = 3.3 V
		T _a = 55°C		1.0	_		RCR3.RTCDV[2:0] set to low drive capacity
		T _a = 85°C		1.1	_		
		T _a = 25°C		1.5	_		VBATT = 2.0 V
		T _a = 55°C		1.8	_		RCR3.RTCDV[2:0] set to normal drive
		T _a = 85°C		2.1	_		Capacity
		T _a = 25°C		1.6	_		VBATT = 3.3 V
		T _a = 55°C		1.9	_	RCF _ capa	RCR3.RTCDV[2:0] set to normal drive
		T _a = 85°C		2.2	_		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.



Figure 2.6 Temperature Dependency of RTC Operation with VCC Off (Reference Data)

Table 2.10DC Characteristics (8)

```
Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V
```

Item	Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Permissible total power consumption*1	Pd	_	_	350	mW	D-version product

Note 1. Total power dissipated by the entire chip (including output currents)



Table 2.11DC Characteristics (9)

Conditions: $1.8 V \le VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF \le 3.6 V$, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, $T_a = -40$ to $+85^{\circ}C$

	ltem	Symbol	Min.	Typ.* ⁷	Max.	Unit	Test Conditions
Analog power	During A/D conversion (at high-speed conversion)	I _{AVCC}		0.7	1.7	mA	
supply current	During A/D conversion (in low-current mode)			0.6	1.0		
	During D/A conversion (per channel)*1			0.4	0.8		
	Waiting for A/D and D/A conversion (all units)			—	0.4	μA	
Reference	During A/D conversion (at high-speed conversion)	I _{REFH0}		25	150	μA	
power supply	Waiting for A/D conversion (all units)			—	60	nA	
current	During D/A conversion (per channel)	I _{REFH}		50	100	μA	
	Waiting for D/A conversion (all units)		_	—	100	nA	
LVD1	—	I _{LVD}	_	0.15	_	μA	
Temperature sensor* ⁶	_	I _{TEMP}		75		μA	
Comparator B	Window mode	I _{CMP} *5	_	12.5	28.6	μA	
operating	Comparator high-speed mode (per channel)		_	3.2	16.2	μA	
	Comparator low-speed mode (per channel)		_	1.7	4.4	μA	
CTSU operating current	 When sleep mode Base clock frequency: 2MHz Pin capacitance: 50pF 	I _{CTSU}		150	_	μA	
USB operating current*4 During USB communication operation under the following settings and conditions • Host controller operation is set to full-speed mode Bulk OUT transfer (64 bytes) × 1, bulk IN transfer (64 bytes) × 1 • Connect peripheral devices via a 1-meter USB colored to the top operation		I _{USBH} *2	_	4.3 (VCC) 0.9 (VCC_USB)		mA	
	 During USB communication operation under the following settings and conditions Function controller operation is set to full-speed mode Bulk OUT transfer (64 bytes) × 1, bulk IN transfer (64 bytes) × 1 Connect the host device via a 1-meter USB cable from the USB port. 	I _{USBF} *2		3.6 (VCC) 1.1 (VCC_USB)	_	mA	
	 During suspended state under the following setting and conditions Function controller operation is set to full-speed mode (pull up the USB0_DP pin) Software standby mode Connect the host device via a 1-meter USB cable from the USB port. 	I _{SUSP} *3	_	0.35 (VCC) 170 (VCC_USB)		μA	

Note 1. The value of the D/A converter is the value of the power supply current including the reference current.

Note 2. Current consumed only by the USB module.

Note 3. Includes the current supplied from the pull-up resistor of the USB0_DP pin to the pull-down resistor of the host device, in addition to the current consumed by this MCU during the suspended state.

Note 4. Current consumed by the power supplies (VCC and VCC_USB).

Note 5. Current consumed only by the comparator B module.

Note 6. Current consumed by the power supply (VCC).

Note 7. When VCC = AVCC0 = VCC_USB = 3.3 V.



Table 2.12DC Characteristics (10)

Conditions: VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF = 3.3 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, $T_a = +25^{\circ}C$

		Тур.			
Item	Symbol	Transmit or	utput power	Unit	Test Conditions
		0 dBm	4 dBm		
BLE operating current	ldd_tx	4.3	8.7	mA	Transmit mode, 2Mbps
(when the DC-to-DC converter is selected)					Transmit mode, 1Mbps
selectery		4.5	8.7		Transmit mode, 500kbps
					Transmit mode, 125kbps
	ldd_rx	3.0	3.5	mA	Receive mode, 2Mbps Prf = –67dBm
		3.0	3.4		Receive mode, 1Mbps Prf = –67dBm
		3.2	3.5		Receive mode, 500kbps Prf = –72dBm
		3.3	3.5		Receive mode, 125kbps Prf = –79dBm
	ldd_idle	0.5		mA	Idle mode
	ldd_slp	1.5		μA	Deep sleep mode
	ldd_down	0.	.1	μA	Power down mode
BLE operating current	ldd_tx	10.2	18.1	mA	Transmit mode, 2Mbps
(when the linear regulator is selected)					Transmit mode, 1Mbps
					Transmit mode, 500kbps
					Transmit mode, 125kbps
	ldd_rx	6.	9	mA	Receive mode, 2Mbps Prf = –67dBm
		6.	9		Receive mode, 1Mbps Prf = –67dBm
		6	9		Receive mode, 500kbps Prf = –72dBm
		7.	1		Receive mode, 125kbps Prf = –79dBm
	ldd_idle	0.	7	mA	Idle mode
	ldd_slp	1.	5	μA	Deep sleep mode
	ldd_down	0.	1	μA	Power down mode

Table 2.13DC Characteristics (11)

Conditions: $1.8 \text{ V} \le \text{VCC} = \text{VCC}_{\text{USB}} = \text{AVCC0} = \text{VCC}_{\text{RF}} = \text{AVCC}_{\text{RF}} \le 3.6 \text{ V}, \text{VSS} = \text{AVSS0} = \text{VSS}_{\text{USB}} = \text{VSS}_{\text{RF}} = 0 \text{ V}, \text{T}_{a} = -40 \text{ to } +85^{\circ}\text{C}$

Item	Symbol	Min.	Тур.	Max.	Unit	Test Conditions
RAM standby voltage	V _{RAM}	1.8	_		V	

Table 2.14DC Characteristics (12)

Conditions: $0 V \le VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF \le 3.6 V$, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, $T_a = -40$ to $+85^{\circ}C$

Item			Min.	Тур.	Max.	Unit	Test Conditions
Power-on VCC rising	At normal startup*1	SrVCC	0.02	-	20	ms/V	
gradient	During fast startup time*2		0.02	_	2		
	Voltage monitoring 0 reset enabled at startup ^{*3, *4}		0.02	_	—		

Note 1. When OFS1.(FASTSTUP, LVDAS) bits are 11b.

Note 2. When OFS1.(FASTSTUP, LVDAS) bits are 01b.

Note 3. When OFS1.LVDAS bit is 0.

Note 4. Turn on the power supply voltage according to the normal startup rising gradient because the settings in the OFS1 register are not read in boot mode.

Table 2.15DC Characteristics (13)

Conditions: $1.8 \text{ V} \le \text{VCC} = \text{VCC}_{\text{USB}} = \text{AVCC0} = \text{VCC}_{\text{RF}} = \text{AVCC}_{\text{RF}} \le 3.6 \text{ V}, \text{VSS} = \text{AVSS0} = \text{VSS}_{\text{USB}} = \text{VSS}_{\text{RF}} = 0 \text{ V}, \text{T}_{a} = -40 \text{ to } +85^{\circ}\text{C}$

The ripple voltage must meet the allowable ripple frequency $f_{r (VCC)}$ within the range between the VCC upper limit and lower limit. When VCC change exceeds VCC ±10%, the allowable voltage change rising/falling gradient dt/dVCC must be met.

Item	Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Allowable ripple frequency	f _{r (VCC)}			10	kHz	Figure 2.7 $V_{r (VCC)} \le VCC \times 0.2$
		_	_	1	MHz	Figure 2.7 $V_{r (VCC)} \le VCC \times 0.08$
		_	_	10	MHz	Figure 2.7 $V_{r (VCC)} \le VCC \times 0.06$
Allowable voltage change rising/falling gradient	dt/dVCC	1.0		—	ms/V	When VCC change exceeds VCC ±10%



Figure 2.7 Ripple Waveform

Table 2.16DC Characteristics (14)

Conditions: $1.8 V \le VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF \le 3.6 V$, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, $T_a = -40$ to +85°C

Item	Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Permissible error of VCL pin external capacitance	C _{VCL}	1.4	4.7	7.0	μF	

Note: The recommended capacitance is 4.7 µF. Variations in connected capacitors should be within the above range.



Table 2.17 Permissible Output Currents

Conditions: 1.8 V \leq VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF \leq 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, T_a = -40 to +85°C

	Item							
Permissible output low current	Ports 03, 05, 07, ports 36, 37,	ports 40 to 47	I _{OL}	4.0	mA			
(average value per pin)	Ports other than above	Normal output mode		4.0				
		High-drive output mode		8.0				
Permissible output low current	Ports 03, 05, 07, ports 36, 37,	ports 40 to 47		4.0				
(maximum value per pin)	Ports other than above	Normal output mode		4.0				
		High-drive output mode		8.0				
Permissible output low current	Total of ports 03, 05, 07, ports	40 to 47	ΣI_{OL}	40				
	Total of ports 14 to 17, ports 2 to 37, port PJ3		40					
	Total of ports B0, B1, B3, B5, B		40					
	Total of port D3, ports E0 to E4	Total of port D3, ports E0 to E4						
	Total of all output pins		80					
Permissible output high current	Ports 03, 05, 07, ports 36, 37,	I _{ОН}	-4.0					
(average value per pin)	Ports other than above	Normal output mode		-4.0				
		High-drive output mode		-8.0				
Permissible output high current	Ports 03, 05, 07, ports 36, 37,	Ports 03, 05, 07, ports 36, 37, ports 40 to 47						
(maximum value per pin)	Ports other than above	Normal output mode		-4.0				
		High-drive output mode		-8.0				
Permissible output high current	Total of ports 03, 05, 07, ports	40 to 47	Σl _{OH}	-40				
	Total of ports 14 to 17, ports 2 to 37, port PJ3	_	-40					
	Total of ports B0, B1, B3, B5, B		-40					
	Total of port D3, ports E0 to E4		-40					
	Total of all output pins	Total of all output pins						

Note: Do not exceed the permissible total supply current.



Table 2.18 Output Values of Voltage (1)

Conditions: 1.8 V \leq VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF \leq 2.7 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, T_a = -40 to +85°C

Item					Min.	Max.	Unit	Test Conditions
Output low	All output ports*1	Normal output	nal output mode		—	0.8	V	I _{OL} = 0.5 mA
		High-drive output mode			—	0.8		I _{OL} = 1.0 mA
Output high	All output ports*1	Normal output mode	Ports 03, 05, 07, Ports 40 to 47	V _{OH}	AVCC0 - 0.5	_	V	I _{OH} = -0.5 mA
			Ports other than above		VCC - 0.5	_		
		High-drive outp	out mode		VCC - 0.5	_		I _{OH} = -1.0 mA

Note 1. This excludes the CLKOUT_RF pin.

Table 2.19Output Values of Voltage (2)

Conditions: $2.7 \text{ V} \le \text{VCC} = \text{VCC}_{\text{USB}} = \text{AVCC0} = \text{VCC}_{\text{RF}} = \text{AVCC}_{\text{RF}} \le 3.6 \text{ V}, \text{VSS} = \text{AVSS0} = \text{VSS}_{\text{USB}} = \text{VSS}_{\text{RF}} = 0 \text{ V}, \text{T}_{a} = -40 \text{ to } +85^{\circ}\text{C}$

Item				Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output ports (except for RIIC) *1	Normal output mode		V _{OL}	_	0.8	V	I _{OL} = 1.0 mA
		High-drive output mode			_	0.8		I _{OL} = 2.0 mA
	RIIC pins	Standard mode (Normal output mode)			_	0.4		I _{OL} = 3.0 mA
		Fast mode (High-drive output mode)			_	0.6		I _{OL} = 6.0 mA
Output high	All output ports*1	Normal output mode	Ports 03, 05, 07, Ports 40 to 47	V _{OH}	AVCC0 - 0.8	_	V	I _{OH} = -1.0 mA
			Ports other than above		VCC – 0.8	_		
		High-drive output mode			VCC - 0.8	_		I _{OH} = -2.0 mA

Note 1. This excludes the CLKOUT_RF pin.

Table 2.20Output Values of Voltage (3)

Conditions: $3.0V \le VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF \le 3.6V$, VSS = AVSS0 = VSS_USB = VSS_RF = 0V, Ta = -40 to +85°C

Item			Min.	Max.	Unit	Test Conditions
Output low	CLKOUT_RF	V _{OL}	_	0.3	V	I _{OL} = 0.5 mA
Output high	CLKOUT_RF	V _{OH}	VCC_RF - 0.3	—	V	I _{OH} = -0.5 mA

2.2.1 Normal I/O Pin Output Characteristics (1)

Figure 2.8 to Figure 2.11 show the characteristics when normal output is selected by the drive capacity control register.



Figure 2.8 V_{OH}/V_{OL} and I_{OH}/I_{OL} Voltage Characteristics at $T_a = 25^{\circ}$ C When Normal Output is Selected (Reference Data)



Figure 2.9 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 1.8 V When Normal Output is Selected (Reference Data)


Figure 2.10 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 2.7 V When Normal Output is Selected (Reference Data)



Figure 2.11 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 3.3 V When Normal Output is Selected (Reference Data)

2.2.2 Normal I/O Pin Output Characteristics (2)

Figure 2.12 to Figure 2.15 show the characteristics when high-drive output is selected by the drive capacity control register.







Figure 2.13 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 1.8 V When High-Drive Output is Selected (Reference Data)



Figure 2.14 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 2.7 V When High-Drive Output is Selected (Reference Data)



Figure 2.15 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 3.3 V When High-Drive Output is Selected (Reference Data)

2.2.3 Normal I/O Pin Output Characteristics (3)

Figure 2.16 to Figure 2.18 show the characteristics of the RIIC output pin.



Figure 2.16 V_{OL} and I_{OL} Voltage Characteristics of RIIC Output Pin at T_a = 25°C (Reference Data)



Figure 2.17 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at VCC = 2.7 V (Reference Data)



Figure 2.18 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at VCC = 3.3 V (Reference Data)



2.3 AC Characteristics

2.3.1 Clock Timing

Table 2.21 Operating Frequency Value (High-Speed Operating Mode)

Conditions: $1.8 V \le VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF \le 3.6 V$, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, $T_a = -40$ to +85°C

			VCC							
	Item	Symbol	1.8 V ≤ VCC < 2.4 V	2.4 V ≤ VCC < 2.7 V	2.7 V ≤ VCC ≤ 3.6 V	When USB is in Use*3	Unit			
Maximum	System clock (ICLK)	f _{max}	8	16	54	54	MHz			
operating frequency* ⁴	FlashIF clock (FCLK)*1, *2		8	16	32	32				
nequency	Peripheral module clock (PCLKA)		8	16	54	54				
	Peripheral module clock (PCLKB)		8	16	32	32				
	Peripheral module clock (PCLKD)		8	32	54	54				
	USB clock (UCLK)	f _{usb}	—	—	—	48				

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When FCLK is in use at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note 2. The frequency accuracy of FCLK must be within $\pm 3.5\%$.

Note 3. The VCC_USB range is 3.0 to 3.6 V when the USB clock is in use.

Note 4. The maximum operating frequency listed above does not include errors of the external oscillator and internal oscillator. For details on the range for the guaranteed operation, see Table 2.24, Clock Timing.

Table 2.22 Operating Frequency Value (Middle-Speed Operating Mode)

Conditions: $1.8 \text{ V} \le \text{VCC} = \text{VCC}_{\text{USB}} = \text{AVCC0} = \text{VCC}_{\text{RF}} = \text{AVCC}_{\text{RF}} \le 3.6 \text{ V}, \text{VSS} = \text{AVSS0} = \text{VSS}_{\text{USB}} = \text{VSS}_{\text{RF}} = 0 \text{ V}, \text{T}_{a} = -40 \text{ to } +85^{\circ}\text{C}$

			VCC							
	Item	Symbol	1.8 V ≤ VCC < 2.4 V	2.4 V ≤ VCC < 2.7 V	2.7 V ≤ VCC ≤ 3.6 V	When USB is in Use*3	Unit			
Maximum	System clock (ICLK)	f _{max}	8	12	12	12	MHz			
operating frequency* ⁴	FlashIF clock (FCLK)*1, *2		8	12	12	12				
nequency	Peripheral module clock (PCLKA)		8	12	12	12				
	Peripheral module clock (PCLKB)		8	12	12	12				
	Peripheral module clock (PCLKD)		8	12	12	12				
	USB clock (UCLK)	f _{usb}	—	—	—	48				

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note 2. The frequency accuracy of FCLK must be within $\pm 3.5\%$.

Note 3. The VCC_USB range is 3.0 to 3.6 V when the USB clock is in use.

Note 4. The maximum operating frequency listed above does not include errors of the external oscillator and internal oscillator. For details on the range for the guaranteed operation, see Table 2.24, Clock Timing.



Table 2.23 Operating Frequency Value (Low-Speed Operating Mode)

Conditions: 1.8 V \leq VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF \leq 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, T_a = -40 to +85°C

				VCC				
	Item	Symbol	1.8 V ≤ VCC < 2.4 V	2.4 V ≤ VCC < 2.7 V	2.7 V ≤ VCC ≤ 3.6 V	Unit		
Maximum	System clock (ICLK)	f _{max}	32.768					
operating frequencv* ³	FlashIF clock (FCLK)*1		32.768					
	Peripheral module clock (PCLKA)							
	Peripheral module clock (PCLKB)			32.768				
	Peripheral module clock (PCLKD)*2		32.768					

Note 1. Programming and erasing the flash memory is impossible.

Note 2. The A/D converter cannot be used.

Note 3. The maximum operating frequency listed above does not include errors of the external oscillator. For details on the range for the guaranteed operation, see Table 2.24, Clock Timing.



Table 2.24 **Clock Timing**

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0= VSS_USB = VSS_RF = 0 V, $T_a = -40$ to +85°C

ltem		Symbol	Min.	Тур.	Max.	Unit	Test Conditions
EXTAL external clock input cycle	time	t _{Xcyc}	50		_	ns	Figure 2.19
EXTAL external clock input high p	oulse width	t _{XH}	20			ns	
EXTAL external clock input low p	ulse width	t _{XL}	20	—		ns	
EXTAL external clock rise time		t _{Xr}			5	ns	
EXTAL external clock fall time		t _{Xf}	_	—	5	ns	
EXTAL external clock input wait t	ime*1	t _{XWT}	0.5	_		μs	
Main clock oscillator oscillation $2.4 \le VCC \le 3.6$		f _{MAIN}	1	_	20	MHz	
frequency*2	1.8 ≤ VCC < 2.4		1	_	8		
Main clock oscillation stabilization	n time (crystal)*2	t _{MAINOSC}	_	3	_	ms	Figure 2.20
Main clock oscillation stabilization resonator)*2	t _{MAINOSC}		50	_	μs		
LOCO clock oscillation frequency	f _{LOCO}	3.44	4.0	4.56	MHz		
LOCO clock oscillation stabilization	t _{LOCO}		—	0.5	μs	Figure 2.21	
IWDT-dedicated clock oscillation	f _{ILOCO}	12.75	15	17.25	kHz		
IWDT-dedicated clock oscillation	stabilization time	t _{ILOCO}		_	50	μs	Figure 2.22
Bluetooth-dedicated clock oscillat	tion frequency	f _{BLECK}		32		MHz	
Bluetooth-dedicated low-speed o oscillation frequency	n-chip oscillator	f _{BLELOCO}	_	32.768	_	kHz	
HOCO clock oscillation frequency	/	f _{HOCO}	31.36	32	32.64	MHz	$T_a = 0$ to +85°C
		(32 MHz)	31.04	32	32.96		$T_a = -40 \text{ to } +85^{\circ}\text{C}$
		f _{HOCO}	52.96	54	55.08	MHz	$T_a = 0$ to +85°C
		(54 MHz)	52.38	54	55.62		$T_a = -40 \text{ to } +85^{\circ}\text{C}$
HOCO clock oscillation stabilizati	on time	t _{HOCO}	—	—	30	μs	Figure 2.24
PLL input frequency*3		f _{PLLIN}	4	—	12.5	MHz	
PLL circuit oscillation frequency*3	3	f _{PLL}	24	—	54	MHz	
PLL clock oscillation stabilization	time	t _{PLL}		—	50	μs	Figure 2.25
PLL free-running oscillation frequ	ency	f _{PLLFR}		8	_	MHz	
USBPLL input frequency*5	f _{PLLIN}		6, 8* ⁶		MHz		
USBPLL circuit oscillation freque	f _{PLL}		48* ⁶		MHz		
USBPLL clock oscillation stabilization	t _{PLL}		—	50	μs	Figure 2.25	
Sub-clock oscillator oscillation fre	equency*7	f _{SUB}	—	32.768	—	kHz	
Sub-clock oscillation stabilization	time*4	t _{SUBOSC}	_	0.5	_	s	Figure 2.26

Note 1. Time until the clock can be used after the main clock oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating).

Note 2. Reference values when an 8-MHz resonator is used.

When specifying the main clock oscillator stabilization time, set the MOSCWTCR register with a stabilization time value that is equal to or greater than the resonator-manufacturer-recommended value.

After the MOSCCR.MOSTP bit is changed to enable the main clock oscillator, confirm that the OSCOVFSR.MOOVF flag has become 1, and then start using the main clock.

Note 3. The VCC range should be 2.4 to 3.6 V when the PLL is used.

Note 4. Reference values when a 32.768-kHz resonator is used. After the setting of the SOSCCR.SOSTP bit or RCR3.RTCEN bit is changed to operate the sub-clock oscillator, only start using

the sub-clock after the sub-clock oscillation stabilization wait time that is equal to or greater than the oscillator-manufacturerrecommended value has elapsed.

Note 5. The VCC range should be 3.0 to 3.6 V when the USBPLL is used.

Note 6. The input frequency can be set to 6 or 8 MHz and the oscillation frequency can be set to 48 MHz only.

Note 7. Only 32.768 kHz can be used.





Figure 2.19 EXTAL External Clock Input Timing



Figure 2.20 Main Clock Oscillation Start Timing



Figure 2.21 LOCO Clock Oscillation Start Timing



Figure 2.22 IWDT-Dedicated Clock Oscillation Start Timing









Figure 2.24 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting HOCOCR.HCSTP Bit)



Figure 2.25 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Been Stabled)



Figure 2.26 Sub-Clock Oscillation Start Timing



2.3.2 Reset Timing

Table 2.25 Reset Timing

Conditions: $1.8 V \le VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF \le 3.6 V$, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, $T_a = -40$ to $+85^{\circ}C$

	ltem	Symbol	Min.	Тур.	Max.	Unit	Test Conditions
RES# pulse width	At power-on	t _{RESWP}	3		_	ms	Figure 2.27
	Other than above	t _{RESW}	30		_	μs	Figure 2.28
Wait time after RES#	At normal startup*1	t _{RESWT}		8.5	_	ms	Figure 2.27
cancellation (at power-on)	During fast startup time* ²	t _{RESWT}	—	560		μs	
Wait time after RES# c (during powered-on sta	t _{RESWT}	—	120		μs	Figure 2.28	
Independent watchdog	timer reset period	t _{RESWIW}	—	1	_	IWDT clock cycle	Figure 2.29
Watchdog timer reset p	period	t _{RESWWW}		4	_	PCLKB cycle	
Software reset period	t _{RESWSW}		1	_	ICLK cycle		
Wait time after indeper	t _{RESWT2}	_	300	_	μs		
Wait time after watchdo	t _{RESWT2}		300	_	μs		
Wait time after software	e reset cancellation	t _{RESWT2}	_	170	_	μs	

Note 1. When OFS1.(LVDAS, FASTSTUP) bits are 11b.

Note 2. When OFS1.(LVDAS, FASTSTUP) bits are a value other than 11b.

Note 3. When IWDTCR.CKS[3:0] bits are 0000b.

Note 4. When WDTCR.CKS[3:0] bits are 0001b.



Figure 2.27 Reset Input Timing at Power-On







Figure 2.29 Reset Input Timing (2)



2.3.3 Timing of Recovery from Low Power Consumption Modes

Table 2.26 Timing of Recovery from Low Power Consumption Modes (1)

Conditions: $1.8 \text{ V} \le \text{VCC} = \text{VCC}_\text{USB} = \text{AVCC0} = \text{VCC}_\text{RF} = \text{AVCC}_\text{RF} \le 3.6 \text{ V}, \text{VSS} = \text{AVSS0} = \text{VSS}_\text{USB} = \text{VSS}_\text{RF} = 0 \text{ V}, \text{T}_a = -40 \text{ to } +85^{\circ}\text{C}$

Item					Min.	Тур.	Max.	Unit	Test Conditions
Recovery time from software standby mode* ¹	High-speed mode	Crystal connected to main clock oscillator	Main clock oscillator operating* ²	t _{SBYMC}	—	2	3	ms	Figure 2.30
		External clock input to main clock oscillator	Main clock oscillator operating* ³	t _{SBYEX}	—	35	50	μs	
		Sub-clock oscillator o	t _{SBYSC}		650	800	μs		
		HOCO clock oscillato	r operating	t _{SBYHO}	—	40	55	μs	
		LOCO clock oscillator	r operating	t _{SBYLO}	—	40	55	μs	

Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. When multiple oscillators are operating, the recovery time varies depending on the operating state of the oscillators that are not selected as the system clock source. The above table applies when only the corresponding clock is operating.

Note 2. When the frequency of the crystal is 20 MHz. When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.

Table 2.27 Timing of Recovery from Low Power Consumption Modes (2)

Conditions: $1.8 \text{ V} \le \text{VCC} = \text{VCC}_\text{USB} = \text{AVCC0} = \text{VCC}_\text{RF} = \text{AVCC}_\text{RF} \le 3.6 \text{ V}, \text{VSS} = \text{AVSS0} = \text{VSS}_\text{USB} = \text{VSS}_\text{RF} = 0 \text{ V}, \text{T}_a = -40 \text{ to } +85^{\circ}\text{C}$

Item					Min.	Тур.	Max.	Unit	Test Conditions
Recovery time from software standby mode*1	Middle-speed mode	Crystal connected to main clock oscillator	Main clock oscillator operating* ²	t _{SBYMC}	—	2	3	ms	Figure 2.30
		External clock input	Main clock oscillator and PLL circuit operating* ³	t _{SBYPC}	—	2	3	ms	
		External clock input to main clock	Main clock oscillator operating*4	t _{SBYEX}	—	3	4	μs	
		oscillator	Main clock oscillator and PLL circuit operating ^{*5}	t _{SBYPE}	—	65	85	μs	
		Sub-clock oscillator o	perating	t _{SBYSC}		600	750	μs	
	-	HOCO clock oscillato	r operating* ⁶	t _{SBYHO}		40	50	μs	
		LOCO clock oscillato	r operating	t _{SBYLO}	—	5	7	μs	

Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. When multiple oscillators are operating, the recovery time varies depending on the operating state of the oscillators that are not selected as the system clock source. The above table applies when only the corresponding clock is operating.
 Note 2. When the frequency of the crystal is 12 MHz.

When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.

Note 3. When the frequency of PLL is 12 MHz.

When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.

Note 4. When the frequency of the external clock is 12 MHz.

When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.

Note 5. When the frequency of PLL is 12 MHz.

When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.

Note 6. This is the case when HOCO is selected as the system clock and its frequency division is set to be 8 MHz.



Note 3. When the frequency of the external clock is 20 MHz. When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.

Table 2.28 Timing of Recovery from Low Power Consumption Modes (3)

Conditions: $1.8 \text{ V} \le \text{VCC} = \text{VCC}_{USB} = \text{AVCC0} = \text{VCC}_{RF} = \text{AVCC}_{RF} \le 3.6 \text{ V}, \text{VSS} = \text{AVSS0} = \text{VSS}_{USB} = \text{VSS}_{RF} = 0 \text{ V}, \text{T}_a = -40 \text{ to } +85^{\circ}\text{C}$

Item				Min.	Тур.	Max.	Unit	Test Conditions
Recovery time from software standby mode* ¹	Low-speed mode	Sub-clock oscillator operating	t _{SBYSC}	_	600	750	μs	Figure 2.30

Note 1. The sub-clock continues oscillating in software standby mode during low-speed mode.



Figure 2.30 Software Standby Mode Recovery Timing

Table 2.29 Timing of Recovery from Low Power Consumption Modes (4)

Conditions: $1.8 \text{ V} \le \text{VCC} = \text{VCC}_{\text{USB}} = \text{AVCC0} = \text{VCC}_{\text{RF}} = \text{AVCC}_{\text{RF}} \le 3.6 \text{ V}, \text{VSS} = \text{AVSS0} = \text{VSS}_{\text{USB}} = \text{VSS}_{\text{RF}} = 0 \text{ V}, \text{T}_{a} = -40 \text{ to } +85^{\circ}\text{C}$

Item		Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Recovery time from deep	High-speed mode*2	t _{DSLP}	—	2	3.5	μs	Figure 2.31
sleep mode*1	Middle-speed mode*3	t _{DSLP}	—	3	4	μs	
	Low-speed mode*4	t _{DSLP}	—	400	500	μs	

Note 1. Oscillators continue oscillating in deep sleep mode.

Note 2. When the frequency of the system clock is 32 MHz.

Note 3. When the frequency of the system clock is 12 MHz.

Note 4. When the frequency of the system clock is 32 kHz.







Table 2.30 Operating Mode Transition Time

Conditions: $1.8 \text{ V} \le \text{VCC} = \text{VCC}_{USB} = \text{AVCC} = \text{VCC}_{RF} = \text{AVCC}_{RF} \le 3.6 \text{ V}, \text{VSS} = \text{AVSS0} = \text{VSS}_{USB} = \text{VSS}_{RF} = 0 \text{ V}, \text{T}_a = -40 \text{ to } +85^{\circ}\text{C}$

Mada before Transition	Mode offer Transition		Tra	Unit		
		ICENTIequency	Min.	Тур.	Max.	Onit
High-speed operating mode	Middle-speed operating modes	8 MHz	—	10	_	μs
Middle-speed operating modes	High-speed operating mode	8 MHz	—	37.5	_	μs
Low-speed operating mode	Middle-speed operating mode, high-speed operating mode	32.768 kHz	—	215	_	μs
Middle-speed operating mode, high-speed operating mode	Low-speed operating mode	32.768 kHz	—	185	_	μs

Note: Values when the frequencies of PCLKA, PCLKB, PCLKD, and FCLK, are not divided.



2.3.4 Control Signal Timing

Table 2.31Control Signal Timing

Conditions: $1.8 V \le VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF \le 3.6 V$, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, $T_a = -40$ to $+85^{\circ}C$

Item	Symbol	Min.	Тур.	Max.	Unit	Test Conditions				
NMI pulse width	t _{NMIW}	200	_	_	ns	NMI digital filter is disabled	t _{Pcyc} × 2 ≤ 200 ns			
		t _{Pcyc} × 2*1	_	—		(NMIFLTE.NFLTEN = 0)	t _{Pcyc} × 2 > 200 ns			
		200	_	—		NMI digital filter is enabled	t _{NMICK} × 3 ≤ 200 ns			
		t _{NMICK} × 3.5* ²	_	—		(NMIFLIE.NFLIEN = 1)	t _{NMICK} × 3 > 200 ns			
IRQ pulse width	t _{IRQW}	200	_	—	ns	IRQ digital filter is disabled	t _{Pcyc} × 2 ≤ 200 ns			
		t _{Pcyc} × 2*1	_	—		(IRQFLIE0.FLIENI = 0)	t _{Pcyc} × 2 > 200 ns			
		200				IRQ digital filter is enabled	t _{IRQCK} × 3 ≤ 200 ns			
		t _{IRQCK} × 3.5* ³	_	—		(IRQFLIE0.FLIENI = 1)	t _{IRQCK} × 3 > 200 ns			

Note: 200 ns minimum in software standby mode.

Note 1. t_{Pcyc} indicates the cycle of PCLKB.

Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.

Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).



Figure 2.32 NMI Interrupt Input Timing







2.3.5 Timing of On-Chip Peripheral Modules

Table 2.32 Timing of On-Chip Peripheral Modules (1)

Conditions: $1.8 \text{ V} \le \text{VCC} = \text{VCC}_{USB} = \text{AVCC0} = \text{VCC}_{RF} = \text{AVCC}_{RF} \le 3.6 \text{ V}, \text{VSS} = \text{AVSS0} = \text{VSS}_{USB} = \text{VSS}_{RF} = 0 \text{ V}, \text{T}_a = -40 \text{ to } +85^{\circ}\text{C}$

	Ite	m		Symbol	Min.	Max.	Unit *1	Test Conditions
I/O ports	Input data pulse width			t _{PRW}	1.5	—	t _{Pcyc}	Figure 2.34
MTU/TPU	Input capture input pulse	width	Single-edge setting	t _{TICW}	1.5	—	t _{Pcyc}	Figure 2.35
			Both-edge setting		2.5	—		
	Timer clock pulse width		Single-edge setting	t _{TCKWH} ,	1.5	_	t _{Pcyc}	Figure 2.36
			Both-edge setting	t _{TCKWL}	2.5	—	-	
			Phase counting mode		2.5	_		
POE	POE# input pulse width		1	t _{POEW}	1.5	_	t _{Pcyc}	Figure 2.37
TMR	Timer clock pulse width	ck pulse width Single-e		t _{TMCWH} ,	1.5	_	t _{Pcyc}	Figure 2.38
			Both-edge setting	t _{TMCWL}	2.5	—	-	
SCI	Input clock cycle time	Input clock cycle time		t _{Scyc}	4	—	t _{Pcyc}	Figure 2.39
			Clock synchronous		6	—	-	
	Input clock pulse width Input clock rise time		1	t _{SCKW}	0.4	0.6	t _{Scvc}	1
				t _{SCKr}	—	20	ns	
	Input clock fall time	put clock fall time		t _{SCKf}	_	20	ns	
	Output clock cycle time Output clock pulse width		Asynchronous	t _{Scvc}	16	—	t _{Pcvc}	Figure 2.40
			Clock synchronous		4	_	,	
			1	t _{SCKW}	0.4	0.6	t _{Scvc}	
Output clock rise time				t _{SCKr}	_	20	ns	
	Output clock fall time		t _{SCKf}	_	20	ns		
	Transmit data delay time (master)	Clock synchro	nous	t _{TXD}	_	40	ns	1
	Transmit data delay time	Clock	2.7 V or above			65	ns	
	(slave)	synchronous	1.8 V or above			100	ns	
	Receive data setup time	Clock	2.7 V or above	t _{RXS}	65	—	ns	
	(master)	synchronous	1.8 V or above		90	—	ns	
	Receive data setup time (slave)	Clock synchron	nous		40	—	ns	
	Receive data hold time	Clock synchro	nous	t _{RXH}	40	_	ns	•
A/D converter	Trigger input pulse width			t _{TRGW}	1.5	_	t _{Pcvc}	Figure 2.41
CAC	CACREF input pulse widt	h	t _{Pcvc} ≤ t _{cac} *2	t _{CACREF}	4.5 t _{cac} + 3 t _{Pcvc}	_	ns	
			$t_{Pcyc} > t_{cac}^{*2}$		5 t _{cac} + 6.5 t _{Pcyc}			
CLKOUT	CLKOUT pin output cycle	*4	VCC = 2.7 V or above	t _{Ccvc}	62.5	_	ns	Figure 2.42
			VCC = 1.8 V or above		125			
	CLKOUT pin high pulse v	vidth ^{*3}	VCC = 2.7 V or above	t _{CH}	15	_	ns	1
			VCC = 1.8 V or above		30			
	CLKOUT pin low pulse w	idth ^{*3}	VCC = 2.7 V or above	t _{CL}	15	_	ns	1
			VCC = 1.8 V or above		30			
	CLKOUT pin output rise t	ime	VCC = 2.7 V or above	t _{Cr}	_	12	ns	1
			VCC = 1.8 V or above			25		
	CLKOUT pin output fall til	me	VCC = 2.7 V or above	e t _{Cf}	_	12	ns	1
			VCC = 1.8 V or above			25		



Table 2.32 **Timing of On-Chip Peripheral Modules (1)**

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, $T_a = -40$ to +85°C

	Item	Symbol	Min.	Max.	Unit *1	Test Conditions
CLKOUT_RF	CLKOUT_RF pin output cycle	t _{CRFcyc}	250	-	ns	Figure 2.43
*5	CLKOUT_RF pin high pulse width	t _{CRFH}	100		ns	
	CLKOUT_RF pin low pulse width CLKOUT_RF pin output rise time CLKOUT_RF pin output fall time		100		ns	
			_	5	ns	
			_	5	ns	

Note 1. t_{Pcyc}: PCLK cycle Note 2. t_{cac}: CAC count clock source cycle

Note 3. When the LOCO is selected as the clock output source (the CKOCR.CKOSEL[2:0] bits are 000b), set the clock output division ratio selection to divided by 2 (the CKOCR.CKODIV[2:0] bits are 001b).

Note 4. When the EXTAL external clock input or an oscillator is used with divided by 1 (the CKOCR.CKOSEL[2:0] bits are 010b and the CKOCR.CKODIV[2:0] bits are 000b) to output from CLKOUT, the above should be satisfied with an input duty cycle of 45 to 55%. Note 5. The voltage for VCC_RF when CLKOUT_RF pin is to be used is between 3.0 V and 3.6 V.



Table 2.33 **Timing of On-Chip Peripheral Modules (2)**

Conditions: $1.8 V \le VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF \le 3.6 V$, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, $T_a = -40$ to +85°C, C = 30 pF, when high-drive output is selected by the drive capacity control register

	Item			Symbol	Min.	Max.	Unit	Test Conditions
P	RSPCK clock	Master		t _{SPcyc}	2	4096	t _{Pcyc} *1	Figure 2.44
	cycle	Slave			8	4096		
	RSPCK clock high pulse width	Master		t _{SPCKWH}	(t _{SPcyc} – t _{SPCKr} – t _{SPCKf})/2 – 3		ns	
		Slave			(t _{SPcyc} – t _{SPCKr} – – – t _{SPCKf})/2			
	RSPCK clock Master			t _{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$		ns	
		Slave			(t _{SPcyc} – t _{SPCKr} – t _{SPCKf})/2	_		
Ī	RSPCK clock	Output	2.7 V or above	t _{SPCKr} ,	_	10	ns	
	rise/fall time		1.8 V or above	t _{SPCKf}		15		
		Input	nput		—	1	μs	-
	Data input setup	Master	2.7 V or above	t _{SU}	10		ns	Figure 2.45
	time		1.8 V or above		30	_		to
		Slave	Slave		25 – t _{Pcvc}			Figure 2.48
-	Data input hold time	Master	RSPCK set to a division ratio other than PCLKB divided by 2	t _H	t _{Pcyc}		ns	
		RSPCK set to PCLKB divided by 2		t _{HF}	0			
	SSL setup time Master			t _H	20 + 2 × t _{Pcvc}	_		
Ī			Master		-30 + N*2 × t _{SPcyc}	_	ns	-
			/e		2	_	t _{Pcyc}	-
-	SSL hold time	Master		t _{LAG}	–30 + N* ³ × t _{SPcyc}	_	ns	
		Slave			2		t _{Pcvc}	
-	Data output	Master 2.7 V or above		t _{OD}	_	14	ns	
	delay time		1.8 V or above		—	30	_	
		Slave	2.7 V or above			3 × t _{Pcvc} + 65		
			1.8 V or above			3 × t _{Pcvc} +105		
	Data output hold	Master		t _{OH}	0		ns	-
	time	Slave			0	_		
-	Successive transmission	Master		t _{TD}	t_{SPcyc} + 2 × t_{Pcyc}	8 × t _{SPcyc} + 2 × t _{Pcvc}	ns	•
	delay time	Slave			4 × t _{Pcvc}			
	MOSI and MISO	Output	2.7 V or above	t _{Dr} , t _{Df}		10	ns	-
rise/fall time			1.8 V or above		—	15		
		Input			—	1	μs	-
ŀ	SSL rise/fall	Output	2.7 V or above	t _{SSLr} ,		10	ns	1
l	time	1.8 V or above		t _{SSLf}		15	ns	-
l		Input	1			1	μs	1
ŀ	Slave access tim	e	2.7 V or above	t _{SA}		6	t _{Pcvc}	Figure 2.47,
			1.8 V or above			7	,.	Figure 2.48
ŀ	Slave output release time		2.7 V or above	t _{REL}	_	5	t _{Pcvc}	1
			1.8 V or above			6	-,0	

Note 1. t_{Pcyc}: PCLK cycle Note 2. N: An integer from 1 to 8 that can be set by the RSPI clock delay register (SPCKD) Note 3. N: An integer from 1 to 8 that can be set by the RSPI slave select negation delay register (SSLND)



Table 2.34Timing of On-Chip Peripheral Modules (3)Conditions: $1.8 V \le VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF \le 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, T_a = -40 to +85°C$

	Item	Symbol	Min.	Max.	Unit* ¹	Test Conditions	
Simple	SCK clock cycle output (master)		t _{SPcyc}	4	65536	t _{Pcyc}	Figure 2.44
SPI	SCK clock cycle input (slave)			6	65536	t _{Pcyc}	
	SCK clock high pulse width		t _{SPCKWH}	0.4	0.6	t _{SPcyc}	
	SCK clock low pulse width		t _{SPCKWL}	0.4	0.6	t _{SPcyc}	
	SCK clock rise/fall time		t _{SPCKr} , t _{SPCKf}	_	20	ns	
	Data input setup time (master)	2.7 V or above	t _{SU}	65	_	ns	Figure 2.45,
		1.8 V or above		95	_		Figure 2.46
	Data input setup time (slave)			40	_		
	Data input hold time	t _H	40	_	ns		
	SSL input setup time	t _{LEAD}	3	_	t _{SPcyc}		
	SSL input hold time		t _{LAG}	3	_	t _{SPcyc}	
	Data output delay time (master)		t _{OD}	_	40	ns	
	Data output delay time (slave)	2.7 V or above		_	65		
		1.8 V or above		_	100		
	Data output hold time (master)	2.7 V or above	t _{ОН}	-10	_	ns	
		1.8 V or above		-20	_		
	Data output hold time (slave)			-10	_		
	Data rise/fall time	t _{Dr} , t _{Df}	_	20	ns		
	SSL input rise/fall time	t _{SSLr} , t _{SSLf}	_	20	ns		
	Slave access time		t _{SA}	_	6	t _{Pcyc}	Figure 2.47,
	Slave output release time		t _{REL}	_	6	t _{Pcyc}	Figure 2.48

Note 1. t_{Pcyc}: PCLK cycle



Table 2.35 **Timing of On-Chip Peripheral Modules (4)**

Conditions: 2.7 V \leq VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF \leq 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, fPCLKB \leq 32 MHz, T_a = -40 to +85°C

Item			Min.*1, *2	Max.	Unit	Test Conditions
RIIC	SCL cycle time	t _{SCL}	6 (12) × t _{IICcyc} + 1300	_	ns	Figure 2.49
(Standard mode SMBus)	SCL high pulse width	t _{SCLH}	3 (6) × t _{IICcyc} + 300	—	ns	
mode, embacy	SCL low pulse width	t _{SCLL}	3 (6) × t _{IICcyc} + 300	_	ns	
	SCL, SDA rise time	t _{Sr}	—	1000	ns	
	SCL, SDA fall time	t _{Sf}	—	300	ns	
	SCL, SDA spike pulse removal time	t _{SP}	0	1 (4) × t _{IICcyc}	ns	
	SDA bus free time	t _{BUF}	3 (6) × t _{IICcyc} + 300	_	ns	
	START condition hold time	t _{STAH}	t _{IICcyc} + 300	_	ns	
	Repeated START condition setup time	t _{STAS}	1000	_	ns	
	STOP condition setup time	t _{STOS}	1000	_	ns	
	Data setup time	t _{SDAS}	t _{IICcyc} + 50	_	ns	
	Data hold time	t _{SDAH}	0	_	ns	
	SCL, SDA capacitive load	Cb	—	400	pF	
RIIC	SCL cycle time	t _{SCL}	6 (12) × t _{IICcyc} + 600	—	ns	Figure 2.49
(Fast mode)	SCL high pulse width	t _{SCLH}	3 (6) × t _{IICcyc} + 300 —		ns	
	SCL low pulse width	t _{SCLL}	3 (6) × t _{IICcyc} + 300	—	ns	
	SCL, SDA rise time	t _{Sr}	—	300	ns	
	SCL, SDA fall time	t _{Sf}	—	300	ns	
	SCL, SDA spike pulse removal time	t _{SP}	0	1 (4) × t _{IICcyc}	ns	
	SDA bus free time	t _{BUF}	3 (6) × t _{IICcyc} + 300	—	ns	
	START condition hold time	t _{STAH}	t _{IICcyc} + 300	—	ns	
	Repeated START condition setup time	t _{STAS}	300	—	ns	
	STOP condition setup time	t _{STOS}	300	—	ns	
	Data setup time	t _{SDAS}	t _{IICcyc} + 50		ns	
	Data hold time	t _{SDAH}	0	_	ns	
	SCL, SDA capacitive load	C _b	_	400	pF	

Note: t_{IICcyc} : RIIC internal reference clock (IIC ϕ) cycle Note 1. The value in parentheses is used when the ICMR3.NF[1:0] bits are set to 11b while a digital filter is enabled with the ICFER.NFE bit = 1.

Note 2. C_b is the total capacitance of the bus lines.

Table 2.36 **Timing of On-Chip Peripheral Modules (5)**

Conditions: 2.7 V \leq VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF \leq 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, fPCLKB \leq 32 MHz, T_a = -40 to +85°C

	Item	Symbol	Min.*1	Max.	Unit	Test Conditions
Simple I ² C	SSDA rise time	t _{Sr}	—	1000	ns	Figure 2.49
(Standard mode)	SSDA fall time	t _{Sf}	-	300	ns	
	SSDA spike pulse removal time	t _{SP}	0	4 × t _{Pcyc}	ns	
	Data setup time	t _{SDAS}	250	_	ns	
	Data hold time	t _{SDAH}	0	_	ns	
	SSCL, SSDA capacitive load	Cb	_	400	pF	
Simple I ² C	SSDA rise time	t _{Sr}	_	300	ns	Figure 2.49
(Fast mode)	SSDA fall time	t _{Sf}	_	300	ns	
	SSDA spike pulse removal time	t _{SP}	0	4 × t _{Pcyc}	ns	
	Data setup time	t _{SDAS}	100		ns	
	Data hold time	t _{SDAH}	0		ns	
	SSCL, SSDA capacitive load	Cb	—	400	pF	

Note: t_{Pcyc} : PCLK cycle Note 1. C_b is the total capacitance of the bus lines.

Table 2.37 **Timing of On-Chip Peripheral Modules (6)**

Conditions: $1.8 \text{ V} \le \text{VCC} = \text{VCC}_{USB} = \text{AVCC0} = \text{VCC}_{RF} = \text{AVCC}_{RF} \le 3.6 \text{ V}, \text{VSS} = \text{AVSS0} = \text{VSS}_{USB} = \text{VSS}_{RF} = 0 \text{ V}, \text{ fPCLKB} \le 32 \text{ MHz}, \text{ T}_a = -40 \text{ to } +85^{\circ}\text{C}$

	Item	Symbol	Min.	Max.	Unit	Test Conditions	
SSI	AUDIO_MCLK input	2.7 V or above	t _{AUDIO}	1	25	MHz	
	frequency	1.8 V or above		1	4		
	Output clock cycle	Output clock cycle			—	ns	Figure 2.50
	Input clock cycle	Input clock cycle			—	ns	
	Clock high level	Clock high level			0.6	to, ti	
	Clock low level	Clock low level			0.6	to, ti	
	Clock rise time	Clock rise time			20	ns	
	Data delay time	2.7 V or above	t _{DTR}	—	65	ns	Figure 2.51
		1.8 V or above		_	105		Figure 2.52
	Setup time	2.7 V or above	t _{SR}	65	—	ns	
		1.8 V or above		90	—		
	Hold time	Hold time			—	ns	
	WS changing edge SSID	WS changing edge SSIDATA output delay			105	ns	Figure 2.53

Table 2.38 **Timing of On-Chip Peripheral Modules (7)**

Conditions: $2.7 \text{ V} \le \text{VCC} = \text{VCC}_\text{USB} = \text{AVCCO} = \text{VCC}_\text{RF} = \text{AVCC}_\text{RF} \le 3.6 \text{ V}, \text{VSS} = \text{AVSSO} = \text{VSS}_\text{USB} = \text{VSS}_\text{RF} = 0 \text{ V},$ fPCLKB $\le 32 \text{ MHz}, T_a = -40 \text{ to } +85^{\circ}\text{C},$ when high-drive output is selected by the drive capacity control register

	Item	Symbol	Min.	Max.	Unit	Test Conditions
SDHI	SDHI_CLK pin output cycle time	t _{PP(SD)}	62.5	-	ns	Figure 2.54
	SDHI_CLK pin output high pulse width	t _{WH(SD)}	18.25		ns	
	SDHI_CLK pin output low pulse width	t _{WL(SD)}	18.25		ns	
	SDHI_CLK pin output rise time	t _{TLH(SD)}		10	ns	
SDHI_CLK pin output fall time		t _{THL(SD)}		10	ns	
	Output data delay time (data transfer mode) for SDHI_CMD and SDHI_D0 to SDHI_D3 pins	t _{ODLY(SD)}	-18.25	18.25	ns	
	Input data setup time for SDHI_CMD and SDHI_D0 to SDHI_D3 pins	t _{ISU(SD)}	9.25	_	ns	
	Input data hold time for SDHI_CMD and SDHI_D0 to SDHI_D3 pins	t _{IH(SD)}	8.3	—	ns	







Figure 2.35 **MTU Input/Output Timing**











Figure 2.38 TMR Clock Input Timing



Figure 2.39 SCK Clock Input Timing









Figure 2.41 A/D Converter External Trigger Input Timing



Figure 2.42 CLKOUT Output Timing







Figure 2.44 RSPI Clock Timing and Simple SPI Clock Timing





















Figure 2.49 RIIC Bus Interface Input/Output Timing and Simple I²C Bus Interface Input/Output Timing







Figure 2.51 SSI Transmission/Reception Timing (SSICR.SCKP=0)







Figure 2.53 SSIDATA Output Delay After SSIWSn Changing Edge



Figure 2.54 SD Host Interface Input/Output Signal Timing

2.4 USB Characteristics

Table 2.39 USB Characteristics (USB0_DP and USB0_DM Pin Characteristics)

Conditions: $3.0 \text{ V} \le \text{VCC} = \text{VCC}_\text{USB} = \text{AVCC} = \text{VCC}_\text{RF} = \text{AVCC}_\text{RF} < 3.6 \text{ V}, \text{VSS} = \text{AVSS0} = \text{VSS}_\text{USB} = \text{VSS}_\text{RF} = 0 \text{ V}, \text{T}_a = -40 \text{ to } +85^{\circ}\text{C}$

	Item		Symbol	Min.	Max.	Unit	Test C	Conditions	
Input	Input high level voltag	je	V _{IH}	2.0	—	V			
characteristics	Input low level voltage	Э	V _{IL}		0.8	V			
	Differential input sense	sitivity	V _{DI}	0.2	_	V	USB0_DP	- USB0_DM	
	Differential common r range	node	V _{CM}	0.8	2.5	V			
Output	Output high level volt	age	V _{OH}	2.8	VCC_USB	V	I _{OH} = -200 µ	IA	
characteristics	Output low level volta	ge	V _{OL}	0.0	0.3	V	I _{OL} = 2 mA		
	Cross-over voltage		V _{CRS}	1.3	2.0	V		Figure 2.55,	
	Rise time	FS	t _r	4	20	ns		Figure 2.56	
		LS		75	300				
	Fall time	FS	t _f	4	20	ns			
		LS		75	300				
	Rise/fall time ratio	FS	t _r /t _f	90	111.11	%	t _r /t _f		
		LS		80	125				
	Output resistance		Z _{DRV}	28	44	Ω	(Adjusting th external eler necessary.)	e resistance by nents is not	
VBUS	VBUS input voltage		V _{IH}	VCC × 0.8	_	V			
characteristics			V _{IL}		VCC × 0.2	V			
Pull-up,	Pull-down resistor		R _{PD}	14.25	24.80	kΩ			
pull-down	Pull-up resistor		R _{PUI}	0.9	1.575	kΩ	During idle s	tate	
			R _{PUA}	1.425	3.09	kΩ	During recep	otion	
Battery	D+ sink current		I _{DP_SINK}	25	175	μA			
Charging Specification	D- sink current		I _{DM_SINK}	25	175	μA			
Ver 1.2	DCD source current		I _{DP_SRC}	7	13	μA			
	Data detection voltag	е	V _{DAT_REF}	0.25	0.4	V			
	D+ source current		V _{DP_SRC}	0.5	0.7	V	Output curre	nt = 250 μA	
	D- source current		V _{DM SRC}	0.5	0.7	V	Output current = 250 µA		



Figure 2.55

USB0_DP and USB0_DM Output Timing







2.5 A/D Conversion Characteristics



Figure 2.57 VREFH0 Voltage Range vs. AVCC0

Table 2.40 A/D Conversion Characteristics (1)

Conditions: 2.7 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0, reference voltage = VREFH0 selected, VSS = AVSS0 = VREFL0 = VSS_USB = VSS_RF = 0 V, T_a = -40 to +85°C

Item		Min.	Тур.	Max.	Unit	Test Conditions
Frequency		1	—	54	MHz	
Resolution			—	12	Bit	
Conversion time*1 (Operation at PCLKD = 54 MHz)	Permissible signal source impedance (Max.)	0.83	—	—	μs	High-precision channel The ADCSR.ADHSC bit is 0 The ADSSTRn register is 0Dh
	= 0.3 KΩ	1.33	_			Normal-precision channel The ADCSR.ADHSC bit is 0 The ADSSTRn register is 28h
Analog input capacitance	Cs		—	15	pF	Pin capacitance included Figure 2.58
Analog input resistance	Rs		—	2.5	kΩ	Figure 2.58
Analog input voltage range	Ain	0	—	VREFH0	V	
Offset error		_	±0.5	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error			±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error			±0.5	—	LSB	
Absolute accuracy			±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential non-linearity error			±1.0	—	LSB	
INL integral non-linearity erro	or	_	±1.0	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential non-linearity error, and INL integral non-linearity error do not include quantization errors.

Table 2.41 A/D Conversion Characteristics (2)

Conditions: 2.4 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, 2.4 V ≤ VREFH0 ≤ AVCC0, reference voltage = VREFH0 selected, VSS = AVSS0 = VREFL0 = VSS_USB = VSS_RF = 0 V, T_a = -40 to +85°C

Item		Min.	Тур.	Max.	Unit	Test Conditions
Frequency		1	—	32	MHz	
Resolution		_	—	12	Bit	
Conversion time ^{*1} (Operation at PCLKD = 32 MHz)	Permissible signal source impedance (Max.) = 1.3 kΩ	1.41	—	—	μs	High-precision channel The ADCSR.ADHSC bit is 0 The ADSSTRn register is 0Dh
		2.25	—	—		Normal-precision channel The ADCSR.ADHSC bit is 0 The ADSSTRn register is 28h
Analog input capacitance	Cs	_	—	15	pF	Pin capacitance included Figure 2.58
Analog input resistance	Rs	_	—	2.5	kΩ	Figure 2.58
Offset error		_	±0.5	±4.5	LSB	
Full-scale error		_	±0.75	±4.5	LSB	
Quantization error		_	±0.5	—	LSB	
Absolute accuracy		-	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential non-linearity	/ error	_	±1.0	—	LSB	
INL integral non-linearity err	or	—	±1.0	±4.5	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential non-linearity error, and INL integral non-linearity error do not include quantization errors.



Table 2.42 A/D Conversion Characteristics (3)

Conditions: 2.7 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0, reference voltage = VREFH0 selected, VSS = AVSS0 = VREFL0 = VSS_USB = VSS_RF = 0 V, T_a = -40 to +85°C

Item		Min.	Тур.	Max.	Unit	Test Conditions
Frequency		1	—	27	MHz	
Resolution		_	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 27 MHz)	Permissible signal source impedance (Max.) = 1.1 kΩ	2	—	—	μs	High-precision channel The ADCSR.ADHSC bit is 1 The ADSSTRn.SST[7:0] bits are 0Dh
		3	—	—		Normal-precision channel The ADCSR.ADHSC bit is 1 The ADSSTRn.SST[7:0] bits are 28h
Analog input capacitance	Cs		—	15	pF	Pin capacitance included Figure 2.58
Analog input resistance	Rs	_	—	2.5	kΩ	Figure 2.58
Offset error		_	±0.5	±4.5	LSB	
Full-scale error		_	±0.75	±4.5	LSB	
Quantization error		_	±0.5	—	LSB	
Absolute accuracy		_	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential non-linearity	/ error	—	±1.0	—	LSB	
INL integral non-linearity error	or	—	±1.0	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential non-linearity error, and INL integral non-linearity error do not include quantization errors.



Table 2.43 A/D Conversion Characteristics (4)

Conditions: $2.4 \text{ V} \le \text{VCC} = \text{VCC}_{USB} = \text{AVCC0} = \text{VCC}_{RF} = \text{AVCC}_{RF} \le 3.6 \text{ V}, 2.4 \text{ V} \le \text{VREFH0} \le \text{AVCC0}, \text{VSS} = \text{AVSS0} = \text{VSS}_{USB} = 0 \text{ V}, \text{ reference voltage} = \text{VREFH0 selected}, \text{T}_{a} = -40 \text{ to } +85^{\circ}\text{C}$

Item		Min.	Тур.	Max.	Unit	Test Conditions
Frequency		1	—	16	MHz	
Resolution		_	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 16 MHz)	Permissible signal source impedance (Max.) = 2.2 kΩ	3.38	—	—	μs	High-precision channel The ADCSR.ADHSC bit is 1 The ADSSTRn register is 0Dh
		5.06	—	—		Normal-precision channel The ADCSR.ADHSC bit is 1 The ADSSTRn register is 28h
Analog input capacitance	Cs	_	—	15	pF	Pin capacitance included Figure 2.58
Analog input resistance	Rs	_	—	2.5	kΩ	Figure 2.58
Offset error		_	±0.5	±4.5	LSB	
Full-scale error		_	±0.75	±4.5	LSB	
Quantization error		_	±0.5	—	LSB	
Absolute accuracy		-	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential non-linearity	/ error	—	±1.0	—	LSB	
INL integral non-linearity err	or	—	±1.0	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential non-linearity error, and INL integral non-linearity error do not include quantization errors.


Table 2.44 A/D Conversion Characteristics (5)

Item		Min.	Тур.	Max.	Unit	Test Conditions
Frequency		1	_	8	MHz	
Resolution			_	12	Bit	
Conversion time*1 (Operation at PCLKD = 8 MHz)	Permissible signal source impedance (Max.) = 5 kΩ	6.75	—	_	μs	High-precision channel The ADCSR.ADHSC bit is 1 The ADSSTRn register is 0Dh
		10.13	—	_		Normal-precision channel The ADCSR.ADHSC bit is 1 The ADSSTRn register is 28h
Analog input capacitance	Cs	_	—	15	pF	Pin capacitance included Figure 2.58
Analog input resistance	Rs		—	2.5	kΩ	Figure 2.58
Offset error		_	±1	±7.5	LSB	
Full-scale error		_	±1.5	±7.5	LSB	
Quantization error			±0.5	-	LSB	
Absolute accuracy			±3.0	±8.0	LSB	
DNL differential non-linearity error		_	±1.0	_	LSB	
INL integral non-linearity err	or	_	±1.25	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential non-linearity error, and INL integral non-linearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 2.45 A/D Converter Channel Classification

Classification	Channel	Conditions	Remarks
High-precision channel	AN000 to AN007	AVCC0 = 1.8 to 3.6 V	Pins AN000 to AN007 cannot be used as digital
Normal-precision channel	AN016 to AN020, AN027		outputs when the A/D converter is in use.
Internal reference voltage input channel	Internal reference voltage	AVCC0 = 2.0 to 3.6 V	
Temperature sensor input channel	Temperature sensor output	AVCC0 = 2.0 to 3.6 V	



Figure 2.58 Equivalent Circuit



Figure 2.59 Illustration of A/D Converter Characteristic Terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of analog input voltage (1-LSB width), that can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and if reference voltage (VREFH0 = 3.072 V), then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, 1.5 mV, ... are used as analog input voltages.

If analog input voltage is 6 mV, absolute accuracy = ± 5 LSB means that the actual A/D conversion result is in the range of 003h to 00Dh, although an output code, 008h, can be expected from the theoretical A/D conversion characteristics.

Integral non-linearity error (INL)

The integral non-linearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential non-linearity error (DNL)

The differential non-linearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

An offset error is the difference between a transition point of the ideal first output code and the actual first output code.

Full-scale error

A full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.



2.6 D/A Conversion Characteristics

Table 2.46D/A Conversion Characteristics (1)

Conditions: $1.8 \text{ V} \le \text{VCC} = \text{VCC}_\text{USB} = \text{AVCC0} = \text{VCC}_\text{RF} = \text{AVCC}_\text{RF} \le 3.6 \text{ V}, \text{VSS} = \text{AVSS0} = \text{VSS}_\text{USB} = \text{VSS}_\text{RF} = 0 \text{ V}, \text{T}_a = -40 \text{ to } +85^{\circ}\text{C}, \text{ Reference voltage} = \text{AVCC0 or AVSS0 selected}$

Item	Min.	Тур.	Max.	Unit	Test Conditions
Resolution	—	—	12	Bit	
Resistive load	30	_	—	kΩ	
Capacitive load	_	_	50	pF	
Output voltage range	0.35	_	AVCC0 - 0.47	V	
DNL differential non-linearity error	_	±0.5	±2.0	LSB	
INL integral non-linearity error	_	±2.0	±8.0	LSB	
Offset error	_	_	±30	mV	
Full-scale error	_	_	±30	mV	
Output resistance	_	5	—	Ω	
Conversion time	_	_	30	μs	

Table 2.47 D/A Conversion Characteristics (2)

Conditions: $1.8 \text{ V} \le \text{VCC} = \text{VCC}_\text{USB} = \text{AVCC0} = \text{VCC}_\text{RF} = \text{AVCC}_\text{RF} \le 3.6 \text{ V}, \text{VSS} = \text{AVSS0} = \text{VSS}_\text{USB} = \text{VSS}_\text{RF} = 0 \text{ V},$ $T_a = -40 \text{ to } +85^{\circ}\text{C}, \text{ Reference voltage = internal reference voltage selected}$

Item	Min.	Тур.	Max.	Unit	Test Conditions
Resolution	—	—	12	Bit	
Internal reference voltage (Vbgr)	1.36	1.43	1.50	V	
Resistive load	30	—	—	kΩ	
Capacitive load	_	—	50	pF	
Output voltage range	0.35	—	Vbgr	V	
DNL differential non-linearity error	_	±2.0	±16.0	LSB	
INL integral non-linearity error	_	±8.0	±16.0	LSB	
Offset error	_	—	30	mV	
Output resistance	_	5	—	Ω	
Conversion time	_	—	30	μs	





Figure 2.60 Illustration of D/A Converter Characteristic Terms

Integral non-linearity error (INL)

The integral non-linearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential non-linearity error (DNL)

The differential non-linearity error is the difference between 1-LSB width based on the ideal D/A conversion characteristics and the width of the actually output code.

Offset error

An offset error is the difference between a transition point of the ideal first output code and the actual first output code.

Full-scale error

A full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.



2.7 Temperature Sensor Characteristics

Table 2.48 Temperature Sensor Characteristics

Conditions: $2.0 \text{ V} \le \text{VCC} = \text{VCC}_{\text{USB}} = \text{AVCC0} = \text{VCC}_{\text{RF}} = \text{AVCC}_{\text{RF}} \le 3.6 \text{ V}, \text{VSS} = \text{AVSS0} = \text{VSS}_{\text{USB}} = \text{VSS}_{\text{RF}} = 0 \text{ V}, \text{T}_{a} = -40 \text{ to } +85^{\circ}\text{C}$

Item	Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Relative accuracy	_	_	±1.5	_	°C	2.4 V or above
		_	±2.0	—		Below 2.4 V
Temperature slope	_	_	-3.65	—	mV/°C	
Output voltage (25°C)	_	_	1.05	—	V	VCC = 3.3 V
Temperature sensor start time	t _{START}	_	—	5	μs	
Sampling time	—	5	—	—	μs	

2.8 Comparator Characteristics

Table 2.49 Comparator Characteristics

Conditions: $1.8 \text{ V} \le \text{VCC} = \text{VCC}_\text{USB} = \text{AVCC0} = \text{VCC}_\text{RF} = \text{AVCC}_\text{RF} \le 3.6 \text{ V}, \text{VSS} = \text{AVSS0} = \text{VSS}_\text{USB} = \text{VSS}_\text{RF} = 0 \text{ V}, \text{T}_a = -40 \text{ to } +85^{\circ}\text{C}$

Item		Symbol	Min.	Тур.	Max.	Unit	Test Conditions
CVREFB2, CVRE	FB3 input reference voltage	VREF	0	—	VCC - 1.4	V	
CMPB2, CMPB3 input voltage		VI	-0.3	—	VCC + 0.3	V	
Offset	Comparator high-speed mode	—	_	—	50	mV	
	Comparator high-speed mode Window function enabled	—	_	—	60	mV	
	Comparator low-speed mode	—	_	—	40	mV	
Comparator output delay time	Comparator high-speed mode	Td	_	—	1.2	μs	VCC = 3 V, input slew rate ≥ 50 mV/µs
	Comparator high-speed mode Window function enabled	Tdw	_	—	2.0	μs	
	Comparator low-speed mode	Td	_	—	5.0	μs	
High-side reference (comparator high-st function enabled)	e voltage speed mode, window	VRFH	_	0.76 VCC	—	V	
Low-side referenc (comparator high- function enabled)	e voltage speed mode, window	VRFL	_	0.24 VCC	_	V	
Operation stabilization	ation wait time	Tcmp	100	—	—	μs	











Comparator Output Delay Time in High-Speed Mode with Window Function Enabled

2.9 CTSU Characteristics

Table 2.50 CTSU Characteristics

Conditions: $1.8 V \le VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF \le 3.6 V$, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, $T_a = -40$ to $+85^{\circ}C$

Item	Symbol	Min.	Тур.	Max.	Unit	Test Conditions
External capacitance connected to TSCAP pin	C _{tscap}	9	10	11	nF	
TS pin capacitive load	C _{base}		_	50	pF	
Permissible output high current	Σl _{OH}		_	-24	mA	When the mutual capacitance method is applied

2.10 Characteristics of Power-On Reset Circuit and Voltage Detection Circuit

Table 2.51 Characteristics of Power-On Reset Circuit and Voltage Detection Circuit (1)

Conditions: $1.8 \text{ V} \le \text{VCC} = \text{VCC}_{\text{USB}} = \text{AVCC0} = \text{VCC}_{\text{RF}} = \text{AVCC}_{\text{RF}} \le 3.6 \text{ V}, \text{VSS} = \text{AVSS0} = \text{VSS}_{\text{USB}} = \text{VSS}_{\text{RF}} = 0 \text{ V}, \text{T}_{a} = -40 \text{ to } +85^{\circ}\text{C}$

Item		Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Voltage detection	Power-on reset (POR)	V _{POR}	1.35	1.50	1.65	V	Figure 2.63, Figure 2.64
level	Voltage detection circuit	V _{det0_1}	2.70	2.82	3.00	V	Figure 2.65
	(LVD0)*1	V _{det0_2}	2.37	2.51	2.67		At falling edge VCC
		V _{det0_3}	1.80	1.90	1.99		
	Voltage detection circuit	V _{det1_4}	2.99	3.10	3.29	V	Figure 2.66
(LVD1)*2	V _{det1_5}	2.89	3.00	3.19		At falling edge VCC	
	V _{det1_6}	2.79	2.90	3.09			
		V _{det1_7}	2.68	2.79	2.98		
		V _{det1_8}	2.57	2.68	2.87		
		V _{det1_9}	2.47	2.58	2.67		
	V _{det1_A}	2.37	2.48	2.57			
	V _{det1_B}	2.10	2.20	2.30			
	V _{det1_C}	1.86	1.96	2.06			
		V _{det1_D}	1.80	1.86	1.96	1	

Note: These characteristics apply when noise is not superimposed on the power supply.

Note 1. n in the symbol Vdet0_n denotes the value of the OFS1.VDSEL[1:0] bits.

Note 2. n in the symbol Vdet1_n denotes the value of the LVDLVLR.LVD1LVL[3:0] bits.



Table 2.52 Characteristics of Power-On Reset Circuit and Voltage Detection Circuit (2)

Conditions: $1.8 V \le VCC0 = VCC_USB = AVCC0 = VCC_RF = AVCC_RF \le 3.6 V$, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, $T_a = -40$ to +85°C

	Item	Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Wait time after	At normal startup*1	t _{POR}	—	9.1	_	ms	Figure 2.64
power-on reset cancellation	During fast startup time ^{*2}	t _{POR}	—	1.6	—		
Wait time after voltage monitoring 0 reset cancellation	Power-on voltage monitoring 0 reset disabled*1	t _{LVD0}	-	568	_	μs	Figure 2.65
	Power-on voltage monitoring 0 reset enabled* ²	-	_	100	_		
Wait time after voltage monitoring 1 reset cancellation		t _{LVD1}	—	100	_	μs	Figure 2.66
Response delay time		t _{det}	—	_	350	μs	Figure 2.63
Minimum VCC down time*3		t _{VOFF}	350	—	—	μs	Figure 2.63, VCC = 1.0 V or above
Power-on reset enable time		t _{W(POR)}	1	—	—	ms	Figure 2.64, VCC = below 1.0 V
LVD operation stabilization time (after LVD is enabled)		Td _(E-A)	—	—	300	μs	Figure 2.66
Hysteresis width (pow	ver-on rest (POR))	V _{PORH}	—	110	—	mV	
Hysteresis width (volta	age detection circuit:	V _{LVH}	—	70	—	mV	When Vdet1_4 is selected
LVD1)			—	60			When Vdet1_5 to Vdet1_9 is selected
			—	50	—		When Vdet1_A or Vdet1_B is selected
			_	40	_		When Vdet1_C or Vdet1_D is selected

Note: These characteristics apply when noise is not superimposed on the power supply.

Note 1. When OFS1.(LVDAS, FASTSTUP) = 11b.

Note 2. When OFS1.(LVDAS, FASTSTUP) ≠ 11b.

Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, and V_{det1} for the POR/LVD.



Figure 2.63 Voltage Detection Reset Timing



Figure 2.64 Power-On Reset Timing



Figure 2.65 Voltage Detection Circuit Timing (Vdet0)





Figure 2.66 Voltage Detection Circuit Timing (V_{det1})

2.11 Oscillation Stop Detection Timing

Table 2.53 Oscillation Stop Detection Timing

```
Conditions: 1.8 V \le VCC = VCC\_USB = AVCC0 = VCC\_RF = AVCC\_RF \le 3.6 V,
VSS = AVSS0 = VREFL0 = VSS_USB = VSS\_RF = 0 V, T_a = -40 to +85°C
```

Item	Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Detection time	t _{dr}	_	_	1	ms	Figure 2.67





2.12 Battery Backup Function Characteristics

Table 2.54 Battery Backup Function Characteristics

Conditions: $1.8 \text{ V} \le \text{VCC} = \text{VCC}_{\text{USB}} = \text{AVCC0} = \text{VCC}_{\text{RF}} = \text{AVCC}_{\text{RF}} \le 3.6 \text{ V}, 1.8 \text{ V} \le \text{VBATT} \le 3.6 \text{ V}, 1.8 \text{ V} \le \text{VBATT} \le 3.6 \text{ V}, 1.8 \text{ V} \le \text{VBATT} \le 3.6 \text{ V}, 1.8 \text{ V} \le \text{VBATT} \le 3.6 \text{ V}, 1.8 \text{ V} \le \text{VBATT} \le 3.6 \text{ V}, 1.8 \text{ V} \le \text{VBATT} \le 3.6 \text{ V}, 1.8 \text{ V} \le \text{VBATT} \le 3.6 \text{ V}, 1.8 \text{ V} \le \text{VBATT} \le 3.6 \text{ V}, 1.8 \text{ V} \le \text{VBATT} \le 3.6 \text{ V}, 1.8 \text{ V} \le \text{VBATT} \le 3.6 \text{ V}, 1.8 \text{ V} \le \text{VBATT} \le 3.6 \text{ V}, 1.8 \text{ V} \le \text{VBATT} \le 3.6 \text{ V}, 1.8 \text{ V} \le \text{VBATT} \le 3.6 \text{ V}, 1.8 \text{ V} \le \text{VBATT} \le 3.6 \text{ V}, 1.8 \text{ V} \le \text{VBATT} \le 3.6 \text{ V}, 1.8 \text{ V} \le 1.8 \text{ V} = 1.8 \text{ V}$

VSS = AVSS0 = VREFL0 = VSS_USB = VSS_RF = 0 V, T_a = -40 to +85°C

Item	Symbol	Min.	Тур.	Max.	Unit	Test Conditions	
Voltage level for switching to battery backup (falling)		V _{DETBATT}	1.99	2.09	2.19	V	Figure 2.68
Hysteresis width	V _{VBATTH}	—	100	—	mV		
VCC-off period for starting power supply switching		t _{VOFFBATT}	—		350	μs	
Allowable voltage change rising/falling gradient		dt/dVCC	1.0		—	ms/V	Figure 2.7
Level for detection of voltage	VBTLVDLVL[1:0] = 10b	V _{DETBATLVD}	2.11	2.20	2.29	V	Figure 2.68
drop on the VBATT pin (falling)	VBTLVDLVL[1:0] = 11b		1.87	2.00	2.13	V	
Hysteresis width for detection of voltage drop on the VBATT pin		V _{BATLVDH}	—	50	—	mV	

Note: The VCC-off period for starting power supply switching indicates the period in which VCC is below the minimum value of the voltage level for switching to battery backup (V_{DETBATT}).



Figure 2.68 Battery Backup Function Characteristics



2.13 ROM (Flash Memory for Code Storage) Characteristics

Table 2.55	ROM (Flash Memory for Code Storage) Characteristics (1)
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Item		Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Reprogramming/erasure cycle*1		N _{PEC}	1000	_	—	Times	
Data hold time	After 1000 times of N_{PEC}	t _{DRP}	20*2, *3		—	Year	T _a = +85°C

Note 1. Definition of reprogram/erase cycle: The reprogram/erase cycle is the number of erasing for each block. When the reprogram/ erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 4-byte programming is performed 256 times for different addresses in a 1-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. Characteristic when using the flash memory programmer and the self-programming library provided from Renesas Electronics. Note 3. This result is obtained from reliability testing.

Table 2.56 ROM (Flash Memory for Code Storage) Characteristics (2) High-Speed Operating Mode

Conditions: $2.7 \text{ V} \le \text{VCC} = \text{VCC}_\text{USB} = \text{AVCC0} = \text{VCC}_\text{RF} = \text{AVCC}_\text{RF} \le 3.6 \text{ V}, \text{VSS} = \text{AVSS0} = \text{VSS}_\text{USB} = 0 \text{ V}$ Temperature range for the programming/erasure operation: $T_a = -40$ to $+85^{\circ}\text{C}$

Itom		Symbol	F	CLK = 1 MF	lz	F	Linit		
nem		Symbol	Min.	Тур.	Max.	Min.	Тур.	Max.	Unit
Programming time	8-byte	t _{P8}	—	112	967	_	52.3	491	μs
Erasure time	2-Kbyte	t _{E2K}	—	8.75	278	_	5.50	215	ms
	512-Kbyte (when block erase command is used)	t _{E512K}	_	928	19218	_	72.0	1679	ms
	512-Kbyte (when all- block erase command is used)	t _{EA512K}	_	923	19013	_	66.7	1469	ms
Blank check time	8-byte	t _{BC8}	_	—	55.0		—	16.1	μs
	2-Kbyte	t _{BC2K}	—	—	1840	_	—	136	ms
Erase operation forced	stop time	t _{SED}	—	—	18.0	_	—	10.7	μs
Start-up area switching	setting time	t _{SAS}	—	12.3	566.5	_	6.2	434	ms
Access window time		t _{AWS}	—	12.3	566.5	—	6.2	434	ms
ROM mode transition wait time 1		t _{DIS}	2.0	—	—	2.0	—	—	μs
ROM mode transition wa	ROM mode transition wait time 2		5.0		_	5.0			μs

Note:The time until each operation of the flash memory is started after instructions are executed by software is not included.Note:The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below

4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of FCLK must be within ±3.5%.



Table 2.57 ROM (Flash Memory for Code Storage) Characteristics (3) Middle-Speed Operating Mode

Conditions: $1.8 \text{ V} \le \text{VCC} = \text{VCC}_\text{USB} = \text{AVCC0} = \text{VCC}_\text{RF} = \text{AVCC}_\text{RF} \le 3.6 \text{ V}, \text{VSS} = \text{AVSS0} = \text{VSS}_\text{USB} = \text{VSS}_\text{RF} = 0 \text{ V}$ Temperature range for the programming/erasure operation: $T_a = -40$ to $+85^{\circ}\text{C}$

Item		Symbol	F	CLK = 1 MH	z	F	Unit		
liem		Symbol	Min.	Тур.	Max.	Min.	Тур.	Max.	Offic
Programming time	8-byte	t _{P8}	_	152	1367	_	97.9	936	μs
Erasure time	2-Kbyte	t _{E2K}	_	8.8	279.7	_	5.9	221	ms
	512-Kbyte (when block erase command is used)	t _{E512K}	_	928	19221	_	191	4108	ms
	512-Kbyte (when all- block erase command is used)	t _{EA512K}	_	923	19015	_	185	3901	ms
Blank check time	8-byte	t _{BC8}		_	85.0	_	_	50.88	μs
	2-Kbyte	t _{BC2K}	_	_	1870	_	_	402	μs
Erase operation forced s	top time	t _{SED}	_		28.0		_	21.3	μs
Start-up area switching setting time		t _{SAS}	_	13.0	573.3		7.7	451	ms
Access window time		t _{AWS}	_	13.0	573.3		7.7	451	ms
ROM mode transition wait time 1		t _{DIS}	2.0		_	2.0	_		μs
ROM mode transition wa	ait time 2	t _{MS}	3.0			3.0		_	μs

Note:The time until each operation of the flash memory is started after instructions are executed by software is not included.Note:The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below

4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set. Note: The frequency accuracy of FCLK must be within ±3.5%.



2.14 E2 DataFlash Characteristics (Flash Memory for Data Storage)

Item		Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Reprogramming/e	erasure cycle* ¹	N _{DPEC}	100000	1000000		Times	
Data hold time	After 10000 times of N _{DPEC}	t _{DDRP}	20*2, *3	_	-	Year	T _a = +85°C
	After 100000 times of N _{DPEC}		5*2, *3	_	_	Year	
	After 1000000 times of N _{DPEC}		_	1* ^{2, *3}		Year	T _a = +25°C

Table 2.58 E2 DataFlash Characteristics (1)

Note 1. The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 100000), erasing can be performed n times for each block. For instance, when 1-byte programming is performed 1000 times for different addresses in a 1-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. Characteristic when the flash memory programmer is used and the self-programming library is provided from Renesas Electronics.

Note 3. These results are obtained from reliability testing.

Table 2.59 E2 DataFlash Characteristics (2): high-speed operating mode

Conditions: $2.7 \text{ V} \le \text{VCC} = \text{VCC}_\text{USB} = \text{AVCC0} = \text{VCC}_\text{RF} = \text{AVCC}_\text{RF} \le 3.6 \text{ V}, \text{VSS} = \text{AVSS0} = \text{VSS}_\text{USB} = \text{VSS}_\text{RF} = 0 \text{ V}$ Temperature range for the programming/erasure operation: $T_a = -40$ to $+85^{\circ}\text{C}$

Item		Symbol	FCL	< = 1 MHz		FCLK	Unit		
		Gymbol	Min.	Тур.	Max.	Min.	Тур.	Max.	Onit
Programming time	1 byte	t _{DP1}		95.0	797	—	40.8	376	μs
Erasure time	1 Kbyte	t _{DE1K}		19.5	498	—	6.2	230	ms
	8 Kbyte	t _{DE8K}		119.8	2556	—	12.9	368	ms
Blank check time	1 byte	t _{DBC1}		—	55.00	—		16.1	μs
	1 Kbyte	t _{DBC1K}		—	0.72	—		0.50	ms
Erase operation forced stop time		t _{DSED}		—	16.0	—		10.7	μs
DataFlash STOP recovery time		t _{DSTOP}	5.0	_	_	5.0	_	_	μs

Note: The time until each operation of the flash memory is started after instructions are executed by software is not included. Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of FCLK must be within $\pm 3.5\%$.

Table 2.60 E2 DataFlash Characteristics (3): middle-speed operating mode

Conditions: $1.8 \text{ V} \le \text{VCC0} = \text{VCC}_\text{USB} = \text{AVCC0} = \text{VCC}_\text{RF} = \text{AVCC}_\text{RF} \le 3.6 \text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS}_\text{USB} = \text{VSS}_\text{RF} = 0 \text{ V}$ Temperature range for the programming/erasure operation: $T_a = -40$ to $+85^{\circ}\text{C}$

ltem		Symbol	FCL	< = 1 MHz		FCL	Unit		
		Symbol	Min.	Тур.	Max.	Min.	Тур.	Max.	Unit
Programming time	1 byte	t _{DP1}		135	1197	_	86.5	823	μs
Erasure time	1 Kbyte	t _{DE1K}		19.6	501	_	8.0	265	ms
	8 Kbyte	t _{DE8K}		120	2558	_	27.7	669	ms
Blank check time	1 byte	t _{DBC1}		—	85.0	_	—	50.9	μs
	1 Kbyte	t _{DBC1K}		—	0.72	_	—	1.45	ms
Erase operation forced stop time		t _{DSED}	-	—	28.0	_	—	21.3	μs
DataFlash STOP recovery time		t _{DSTOP}	0.72	_	—	0.72	_	—	μs

Note:The time until each operation of the flash memory is started after instructions are executed by software is not included.Note:The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below
4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of FCLK must be within ±3.5%.



2.15 BLE Characteristics

2.15.1 Transmission Characteristics

Table 2.61 Transmission Characteristics

Conditions: VCC = VCC_RF = AVCC_RF = 3.3 V, VSS = VSS_RF = 0 V, T_a = $+25^{\circ}\text{C}$

Item	Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Range of frequency	RF _{CF}	2402	—	2480	MHz	
Data rate	RF _{DATA_2M}		2		Mbps	
	RF _{DATA_1M}		1		Mbps	
	RF _{DATA_500k}		500		kbps	
	RF _{DATA_125k}		125		kbps	
Maximum transmitted output	RF _{POWER}		0	2	dBm	0 dBm output mode
power			4	6	dBm	4 dBm output mode
Output frequency error	RF _{TXFERR}	-10	—	10	ppm	*1

Note: The characteristics are based on pins and functions other than those for the BLE interface not being in use.

Note 1. This does not take frequency errors due to manufacturing irregularities, drift with temperature, or deterioration of the crystal over time into account.

2.15.2 Reception Characteristics (2 Mbps)

Table 2.62 Reception Characteristics

Conditions: VCC = VCC_RF = AVCC_RF = 3.3 V, VSS = VSS_RF = 0 V, T_a = +25°C

Item	Symbol	Min.	Тур.	Max.	Unit	Tes	t Conditions
Input frequency	RF _{RXFIN_2M}	2402	_	2480	MHz		
Maximum input level	RF _{LEVL_2M}	-10	4	_	dBm	*1	
Receiver sensitivity	RF _{STY_2M}	_	-92	_	dBm	*1	
Secondary emission strength	RF _{RXSP_2M}	_	-72	-57	dBm	30 MHz to 1 GHz	
		_	-54	-47	dBm	1 GHz to 12 GHz	
Co-channel rejection ratio	RF _{CCR_2M}	_	-8	_	dB	Prf = -67 dBm*1	
Adjacent channel rejection	RF _{ADCR_2M}	_	2	_	dB	Prf = -67 dBm*1	±2 MHz
ratio		_	35	_	dB		±4 MHz
		_	39	_	dB		±6 MHz
Blocking	RF _{BLK_2M}	_	-1	_	dBm	Prf = -67 dBm*1	30 MHz to 2000 MHz
		_	-25	_	dBm		2000 MHz to 2399 MHz
		_	-21	_	dBm		2484 MHz to 3000 MHz
		_	-10	_	dBm		> 3000 MHz
Allowable frequency deviation* ²	RF _{RXFER_2M}	-120	—	120	ppm	*1	
RSSI accuracy	RF _{RSSIS_2M}	_	±4	_	dB	–70 dBm ≤ Prf ≤ -	-10 dBm

Note: The characteristics are based on pins and functions other than those for the BLE interface not being in use.

Note 1. PER \leq 30.8%, and a 37-byte payload

Note 2. Allowable range of difference between the center frequency for the RF input signals and the carrier frequency generated within the chip



2.15.3 Reception Characteristics (1 Mbps)

Table 2.63 Reception Characteristics

Conditions: VCC = VCC_RF = AVCC_RF = 3.3 V, VSS = VSS_RF = 0 V, T_a = +25°C

Item	Symbol	Min.	Тур.	Max.	Unit	Test	t Conditions
Input frequency	RF _{RXFIN_1M}	2402	—	2480	MHz		
Maximum input level	RF _{LEVL_1M}	-10	4	_	dBm	*1	
Receiver sensitivity	RF _{STY_1M}	_	-95	_	dBm	*1	
Secondary emission strength	RF _{RXSP_1M}	_	-72	-57	dBm	30MHz to 1GHz	
		_	-54	-47	dBm	1GHz to 12GHz	
Co-channel rejection ratio	RF _{CCR_1M}	_	-7	_	dB	Prf = -67dBm*1	
Adjacent channel rejection ratio	RF _{ADCR_1M}	_	-1	_	dB	$Prf = -67 dBm^{*1}$	±1MHz
		_	34	_	dB		±2MHz
			35		dB		±3MHz
Blocking	RF _{BLK_1M}	_	0	_	dBm	$Prf = -67 dBm^{*1}$	30MHz to 2000MHz
		_	-24	_	dBm		2000MHz to 2399MHz
		_	-20	_	dBm		2484MHz to 3000MHz
		_	-4	_	dBm		> 3000MHz
Allowable frequency deviation*2	RF _{RXFER_1M}	-120	_	120	ppm	*1	
RSSI accuracy	RF _{RSSIS_1M}	—	±4	_	dB	–70dBm ≤ Prf ≤ –10dBm	

Note: The characteristics are based on pins and functions other than those for the BLE interface not being in use.

Note 1. $PER \le 30.8\%$, and a 37-byte payload

Note 2. Allowable range of difference between the center frequency for the RF input signals and the carrier frequency generated within the chip

2.15.4 Reception Characteristics (500 kbps)

Table 2.64 Reception Characteristics

Conditions: VCC = VCC RF = AVCC RF = 3.3 V, VSS = VSS RF = 0 V, T_a = +25°C

-	—	,	-		a		
Item	Symbol	Min.	Тур.	Max.	Unit	Test	Conditions
Input frequency	RF _{RXFIN_500k}	2402	_	2480	MHz		
Maximum input level	RF _{LEVL_500k}	-10	4	—	dBm	*1	
Receiver sensitivity	RF _{STY_500k}	_	-100	—	dBm	*1	
Secondary emission strength	RF _{RXSP_500k}	_	-72	-57	dBm	30MHz to 1GHz	
			-54	-47	dBm	1GHz to 12GHz	
Co-channel rejection ratio	RF _{CCR_500k}	_	-4	—	dB	$Prf = -72dBm^{*1}$	
Adjacent channel rejection ratio	RF _{ADCR_500k}		6	—	dB	$Prf = -72dBm^{*1}$	±1MHz
		_	36	—	dB		±2MHz
			42	—	dB	-	±3MHz
Blocking	RF _{BLK_500k}		0	—	dBm	$Prf = -72dBm^{*1}$	30MHz to 2000MHz
		_	-23	—	dBm		2000MHz to 2399MHz
			-20	—	dBm	-	2484MHz to 3000MHz
		_	-7	—	dBm		> 3000MHz
Allowable frequency deviation*2	RF _{RXFER_500k}	-120	_	120	ppm	*1	
RSSI accuracy	RF _{RSSIS_500k}	_	±4	—	dB	–70dBm ≤ Prf ≤ –	10dBm

Note: The characteristics are based on pins and functions other than those for the BLE interface not being in use.

Note 1. PER \leq 30.8%, and a 37-byte payload

Note 2. Allowable range of difference between the center frequency for the RF input signals and the carrier frequency generated within the chip



2.15.5 Reception Characteristics (125 kbps)

Table 2.65 Reception Characteristics

Conditions: VCC = VCC_RF = AVCC_RF = 3.3 V, VSS = VSS_RF = 0 V, T_a = +25°C

Item	Symbol	Min.	Тур.	Max.	Unit	Tes	t Conditions	
Input frequency	RF _{RXFIN_125k}	2402	_	2480	MHz			
Maximum input level	RF _{LEVL_125k}	-10	4	_	dBm	*1		
Receiver sensitivity	RF _{STY_125k}		-105	_	dBm	*1		
Secondary emission strength	RF _{RXSP_125k}	_	-72	-57	dBm	30 MHz to 1 GHz		
		_	-54	-47	dBm	1 GHz to 12 GHz		
Co-channel rejection ratio	RF _{CCR_125k}	_	-2	_	dB	Prf = -79 dBm*1		
Adjacent channel rejection ratio	RF _{ADCR_125k}	_	12	_	dB	Prf = -79 dBm*1	±1 MHz	
		_	39	_	dB		±2 MHz	
		_	45	_	dB		±3 MHz	
Blocking	RF _{BLK_125k}	_	0	_	dBm	Prf = -79 dBm*1	30 MHz to 2000 MHz	
		_	-23	_	dBm		2000 MHz to 2399 MHz	
		_	-20	_	dBm		2484 MHz to 3000 MHz	
		_	-1	_	dBm		> 3000MHz	
Allowable frequency deviation*2	$RF_{RXFER_{125k}}$	-120	_	120	ppm	*1		
RSSI accuracy	RF _{RSSIS_125k}	—	±4	_	dB	T_a = +25°C, −70 dBm ≤ Prf ≤ −10 dBm		

Note: The characteristics are based on pins and functions other than those for the BLE interface not being in use.

Note 1. PER ≤ 30.8%, and a 37-byte payload

Note 2. Allowable range of difference between the center frequency for the RF input signals and the carrier frequency generated within the chip



2.16 Usage Notes

2.16.1 Connecting VCL Capacitor and Bypass Capacitors

This MCU integrates an internal voltage-down circuit, which is used for lowering the power supply voltage in the internal MCU automatically to the optimum level. A 4.7- μ F capacitor needs to be connected between this internal voltage-down power supply (VCL pin) and the VSS pin. Place an external capacitor close to the pins. Do not apply the power supply voltage to the VCL pin.

Insert a multilayer ceramic capacitor as a bypass capacitor between each pair of the power supply pins. Implement a bypass capacitor as closer to the MCU power supply pins as possible. We recommend capacitors with a value of 2.2 μ F for that connected to the VCC_RF pin and 0.1 μ F for the others. For the capacitors related to crystal oscillation, see section 9, Clock Generation Circuit in the User's Manual: Hardware. For the capacitors related to analog modules, also see section 44, 12-Bit A/D Converter (S12ADE) in the User's Manual: Hardware.

For notes on designing the printed circuit board, see the descriptions of the application note, the Hardware Design Guide (R01AN1411EJ). The latest version can be downloaded from the Renesas Electronics website.



Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in "Packages" on Renesas Electronics Corporation website.



Figure A 85-Pin BGA (PTBG0085KB-A)





Figure B 56-Pin QFN (PVQN0056LA-A)



REVISION HISTORY RX23W Group Datasheet	REVISION HISTORY	RX23W Grou	p Datasheet
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Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update

- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	Classification
1.00	Aug 06, 2019	_	First edition, issued	

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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